Analog and digital electronics developments

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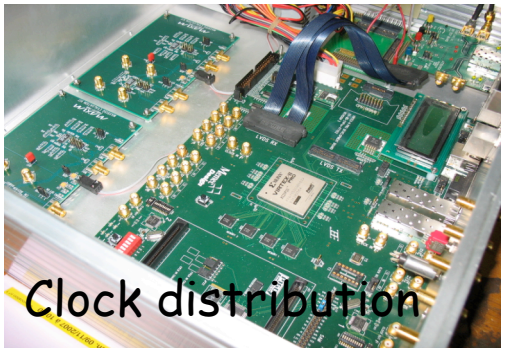

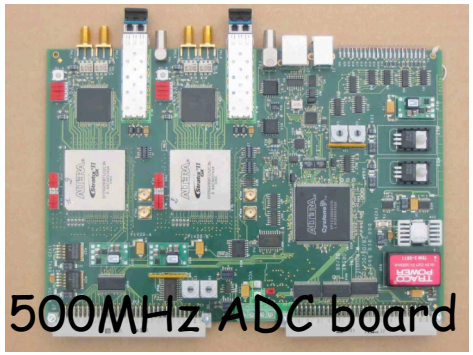

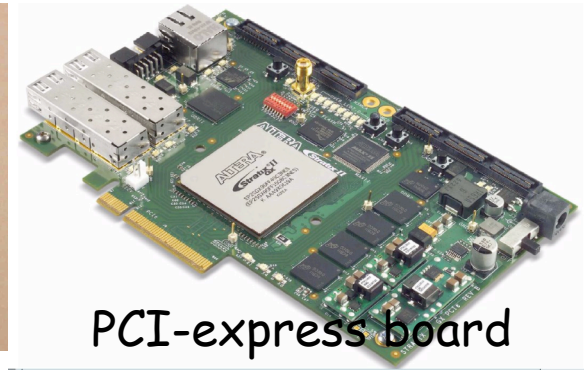

Outline

- Electronics Overview
- Tests in Lab
- Tests in Nançay (NRT)
- Tests in Pittsburgh

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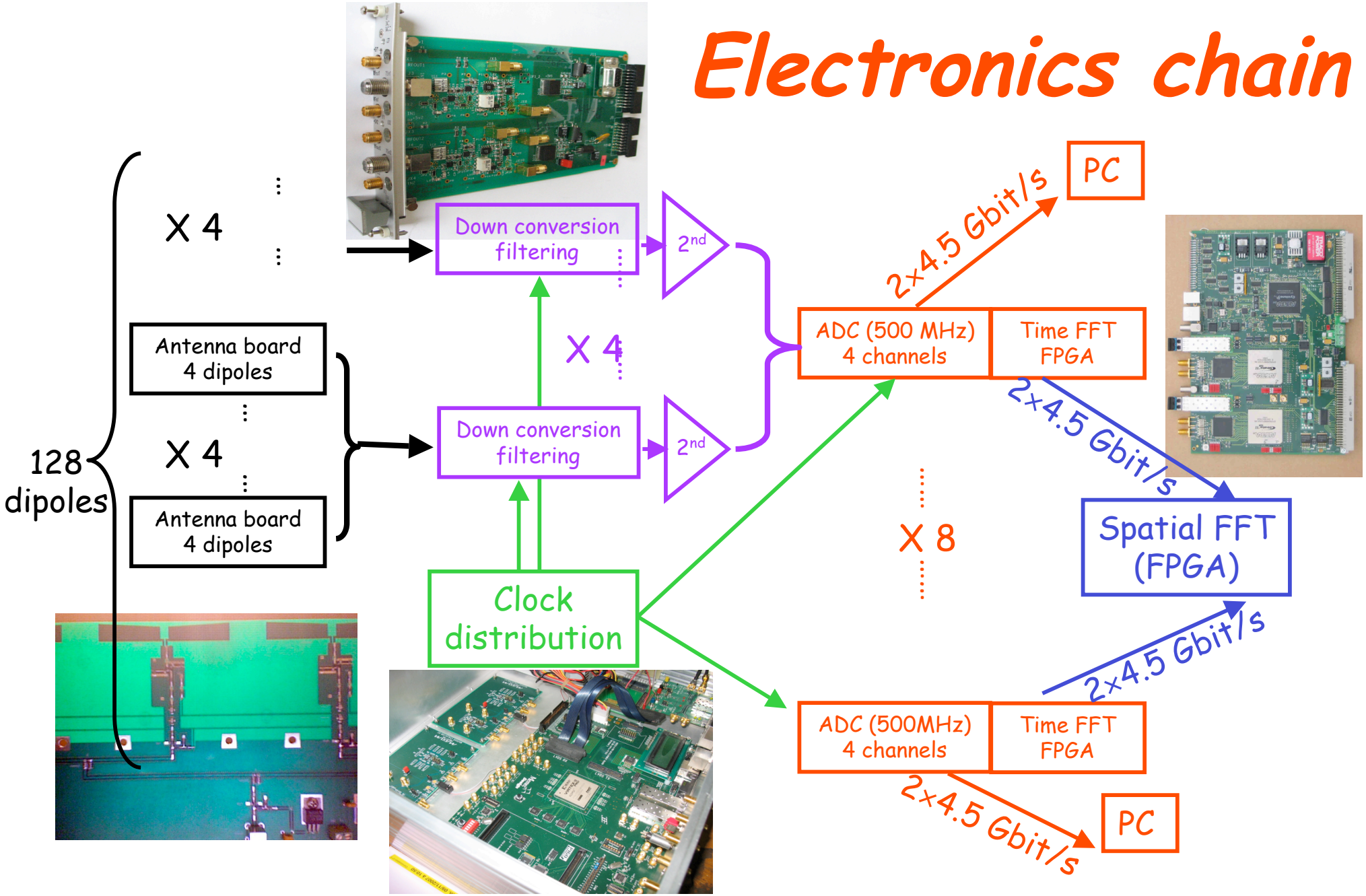
Electronics overview

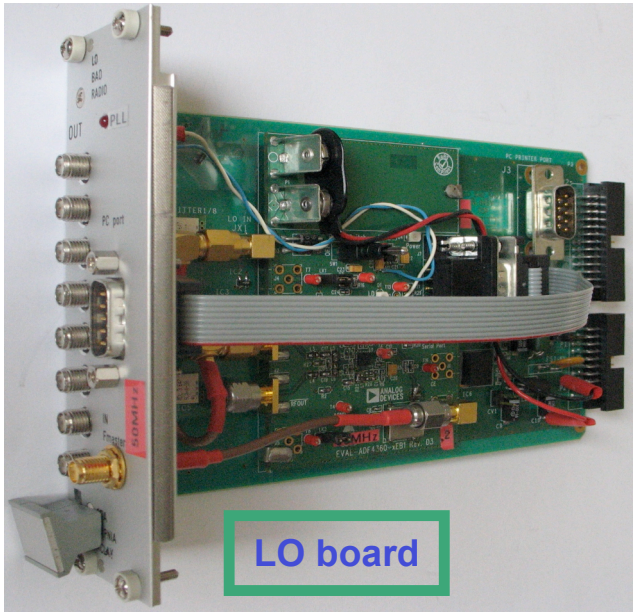
Electronics chain

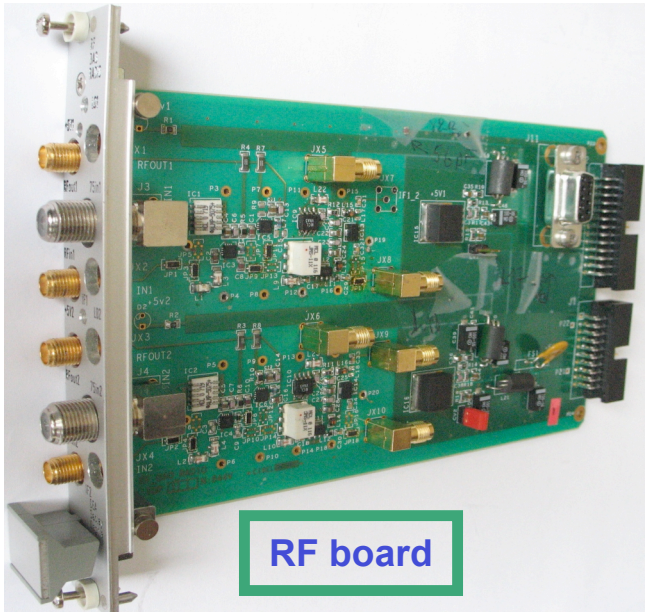


Analog Electronics

Goals:

- Filtering and down conversion: Shift from 1.5 GHz signal to a 0-250 MHz window.
- 2nd stage amplifier up to 650 mV (signal input for ADC)
- Two boards have been developed
  - "LO" board: LO clock and splitter
  - "RF" board: Amplifier + Mixer

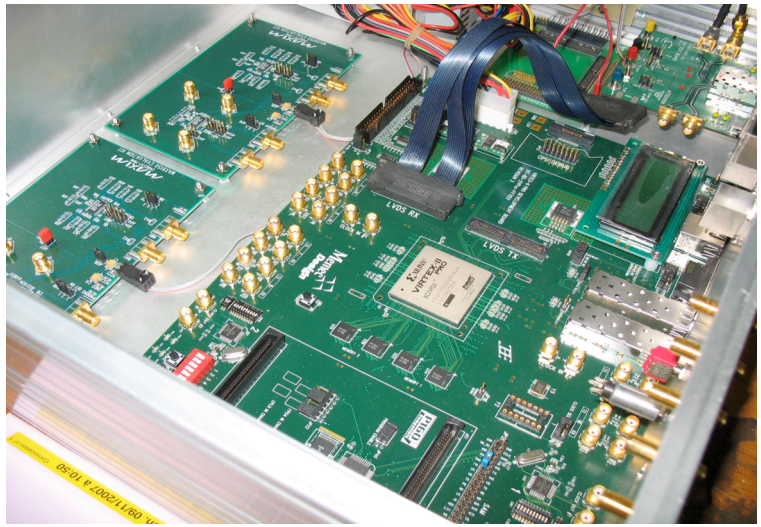




Clock Distribution

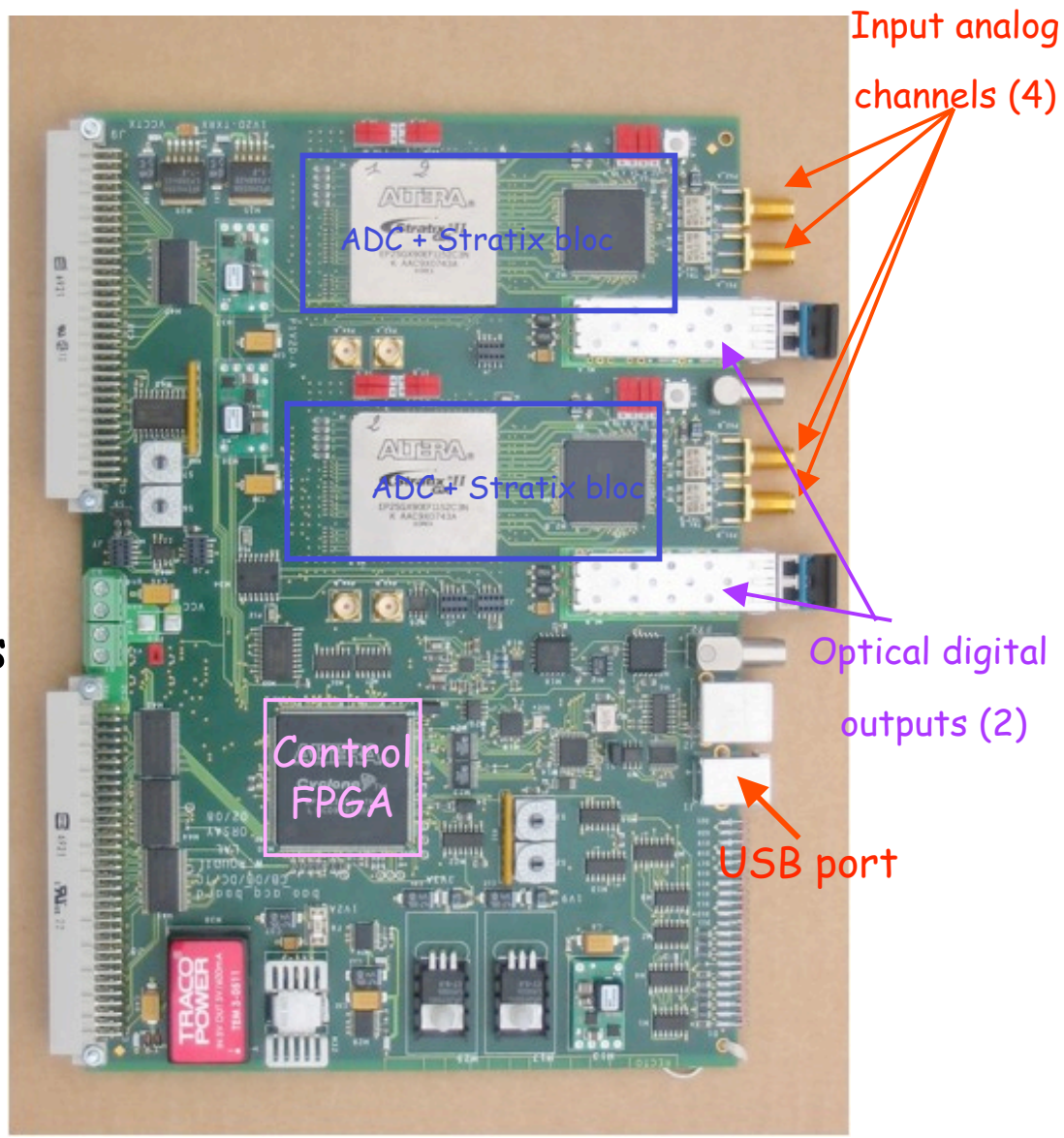
Goals:

- Synchronization of the interferometer clock
- Clock Distribution for ADC boards and for Local Oscillator boards
- Clock & commands encoded on optical fiber (slow-control & configuration capability)
- Define Trigger (Sampling start) and Reset for ADC boards
- Configuration byte transmitted to ADC with trigger (On/Off..)
- Use of external rubidium master clock (specific to Nançay)



500MHz ADC board

- Each ADC board has :
  - 4 input channels (digitized at 500 MHz max)
  - Input clock + control (start/stop…) ports
  - USB, and VME communications port (for control)
  - 2 high speed (4.8 Gbit/s) optical outputs (data links to PCI-express boards)
- Data recorded on fits format on server disk (~200MB/s)



Tests in lab

Method for jitter measurements

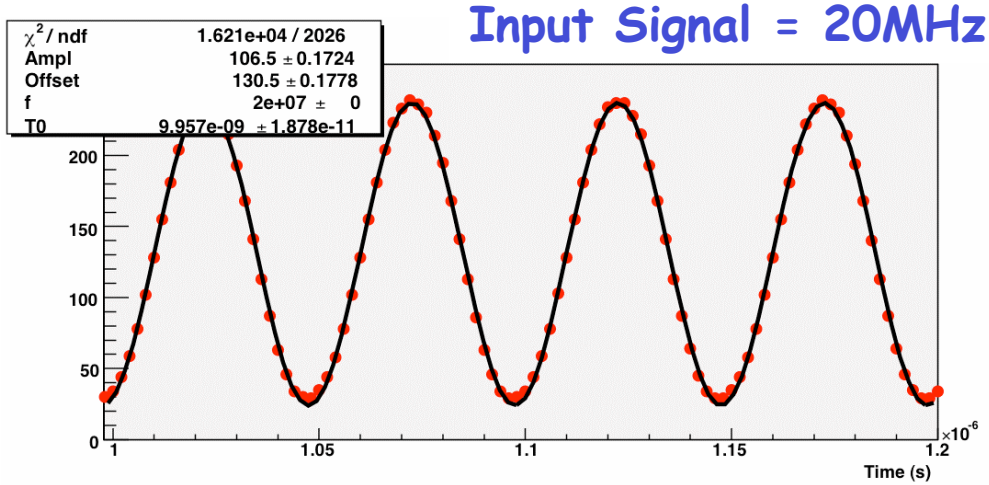
Principle:

- Sine signal split into four "synchronized" input signals
- 4 channels (2 per ADC) measure simultaneously

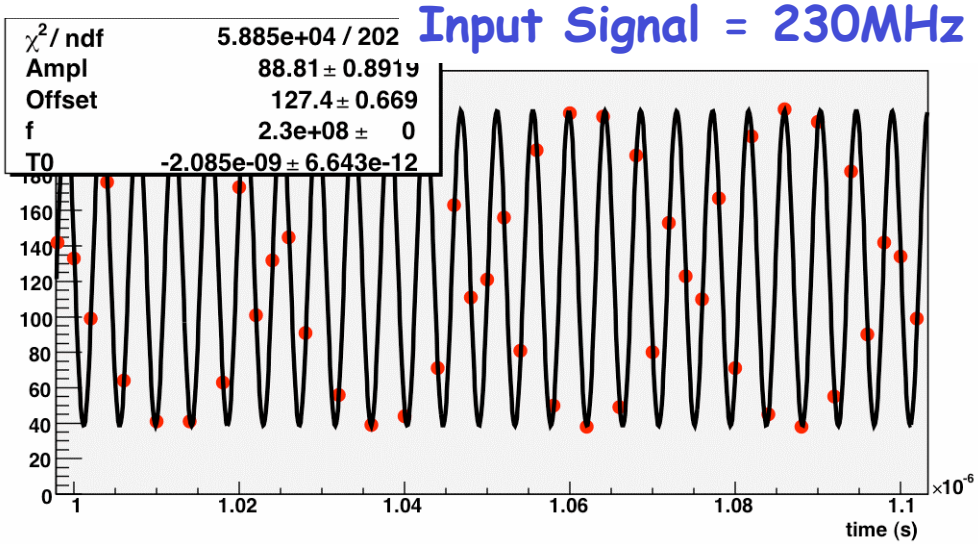
- **Method 1** :Fit of a sine $A(t)= A_0 + A_1 x \sin(2\pi f(i x \Delta t + t_0))$
- The difference of t_0 between channels give the jitter
- **Method 2**: phase difference of the FFT coefficients between channels for the given frequency

- Similar results for the 2 methods
- Frame length : 4k samples

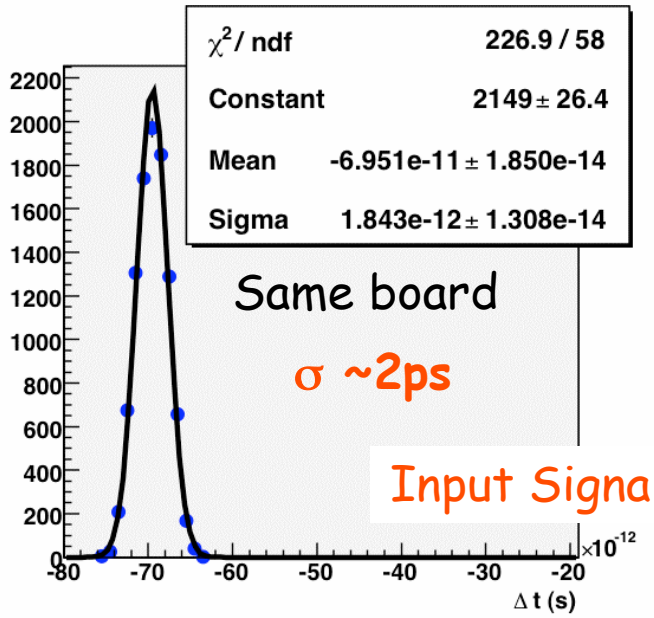
Input Signal = 20MHz

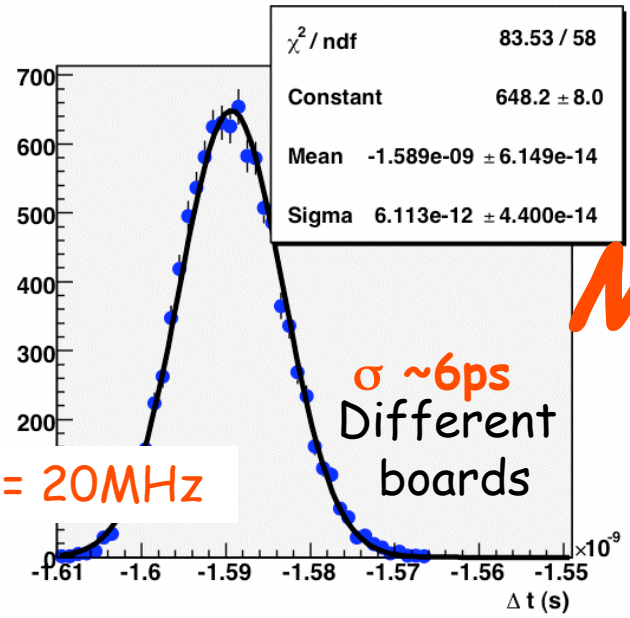


Input Signal = 230MHz

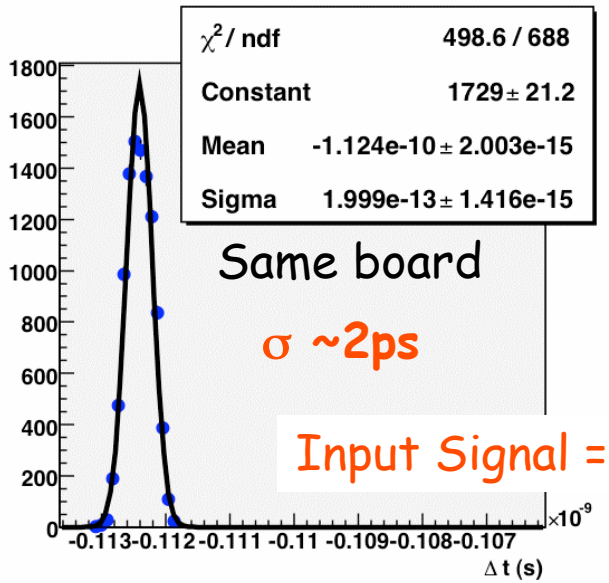


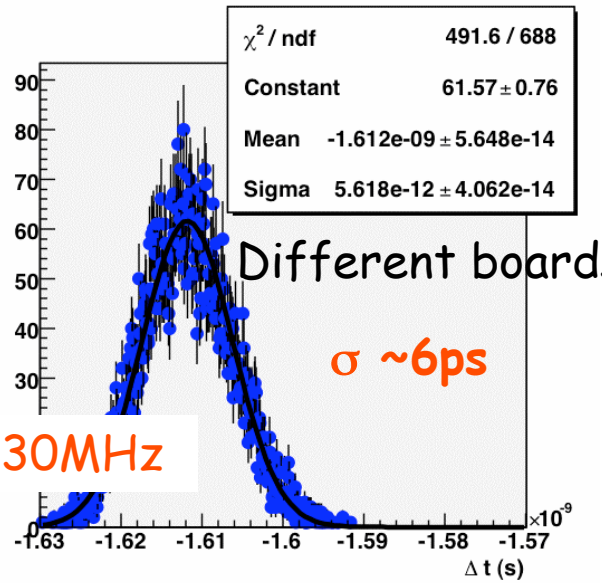
Measurements of Jitter





Input Signal = 20MHz





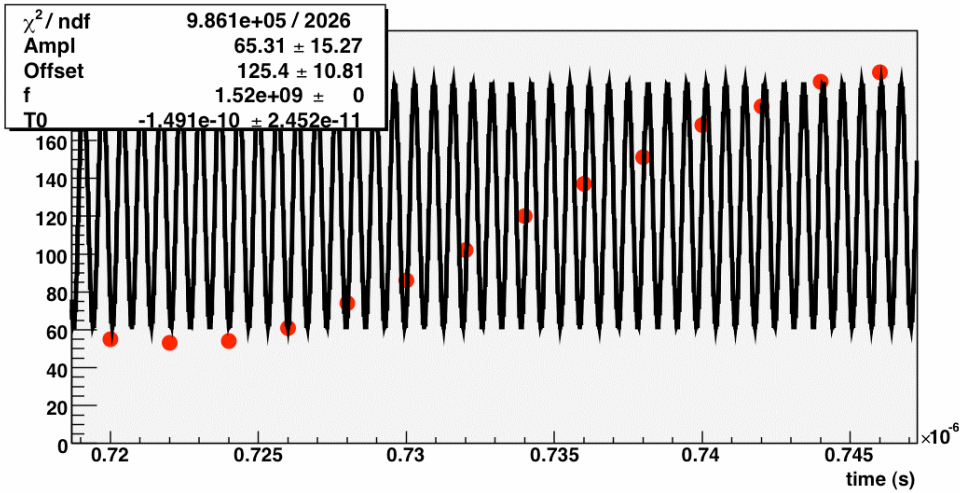
Input Signal = 230MHz

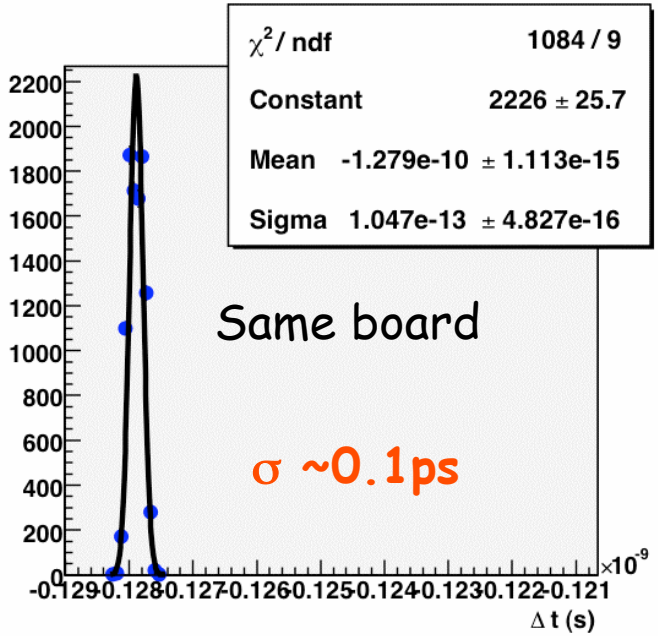
- Lot of work on pll used in ADC board to get a stable 500 MHz clock.
- **Time resolution between channel better than 10 ps.**

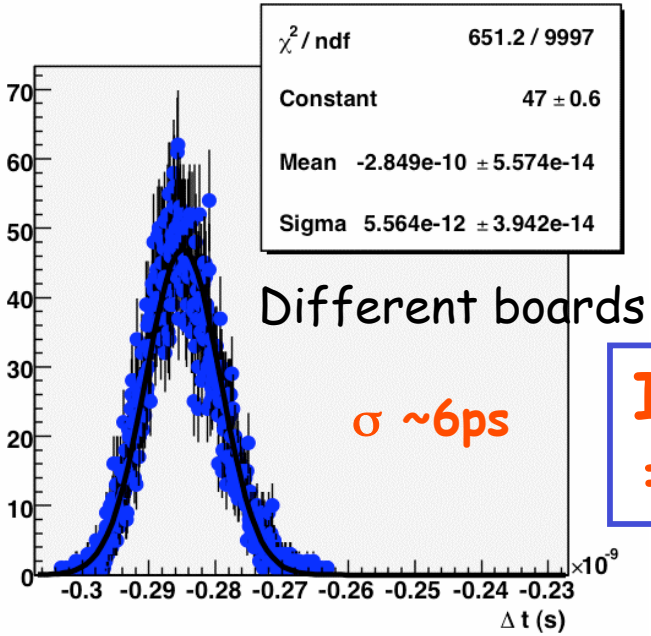
Undersampling: time resolution

Principle:

- Test of the ADC above Nyquist limit (250 MHz) for a sampling at 500MHz.
- Folding of the frequencies 50MHz ⇔ 1050MHz ⇔ 1450MHz ⇔ 1550MHz

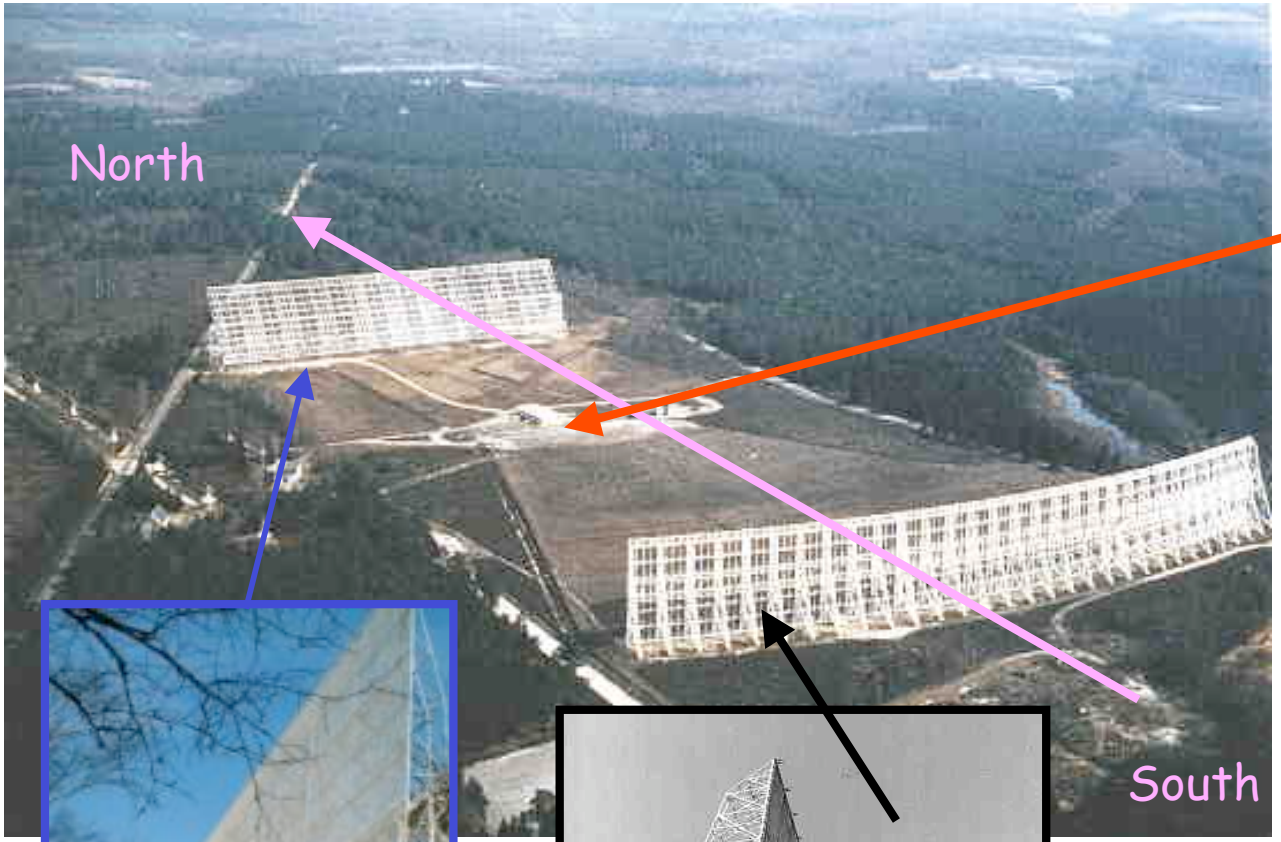






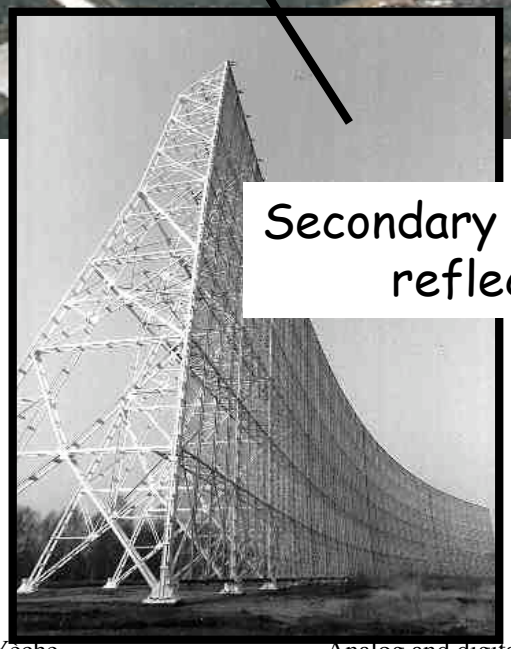
Input Signal = 1520MHz

Test with Nançay Radio Telescope (NRT)



Focal carriage

Primary flat reflector



Secondary spherical reflector

Nançay Radio Telescope

Tests with NRT

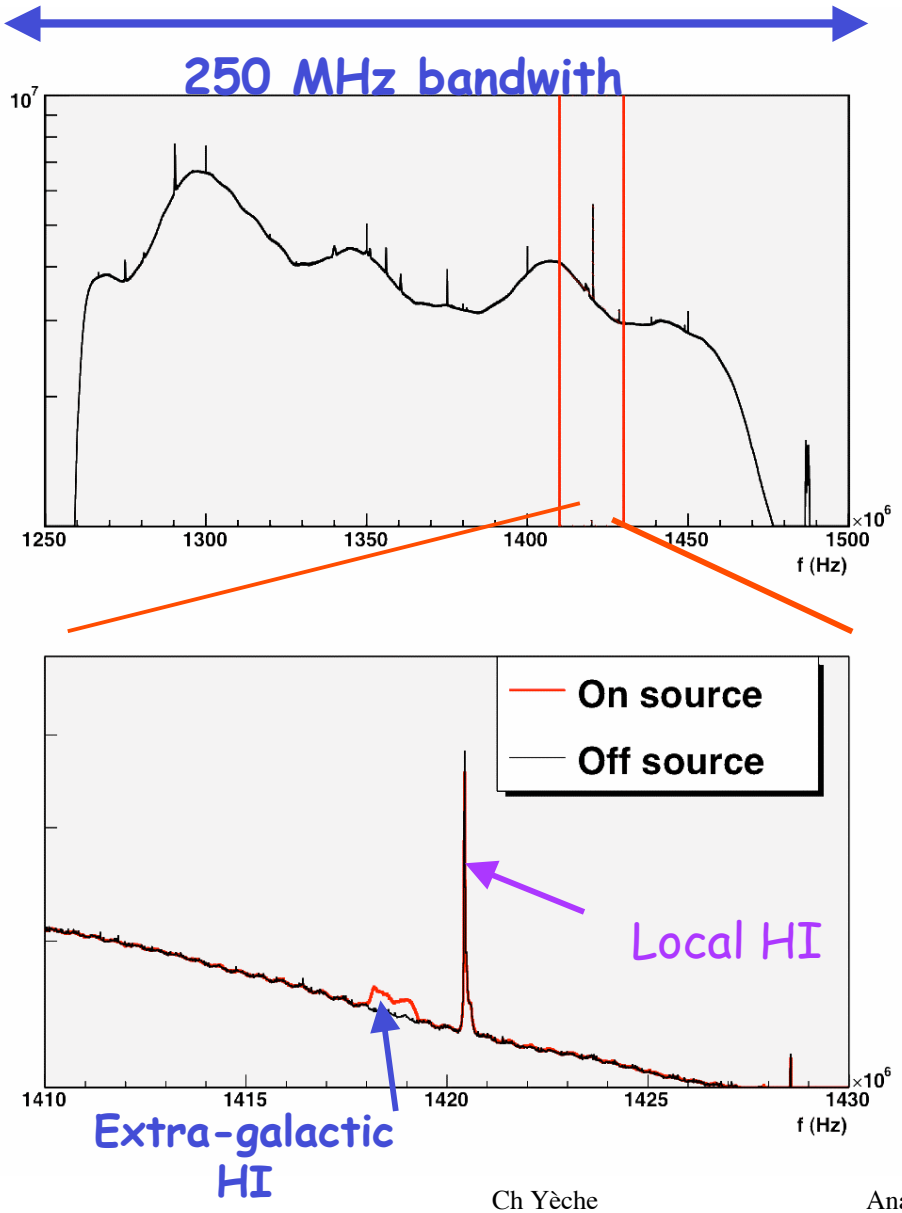
Strategy

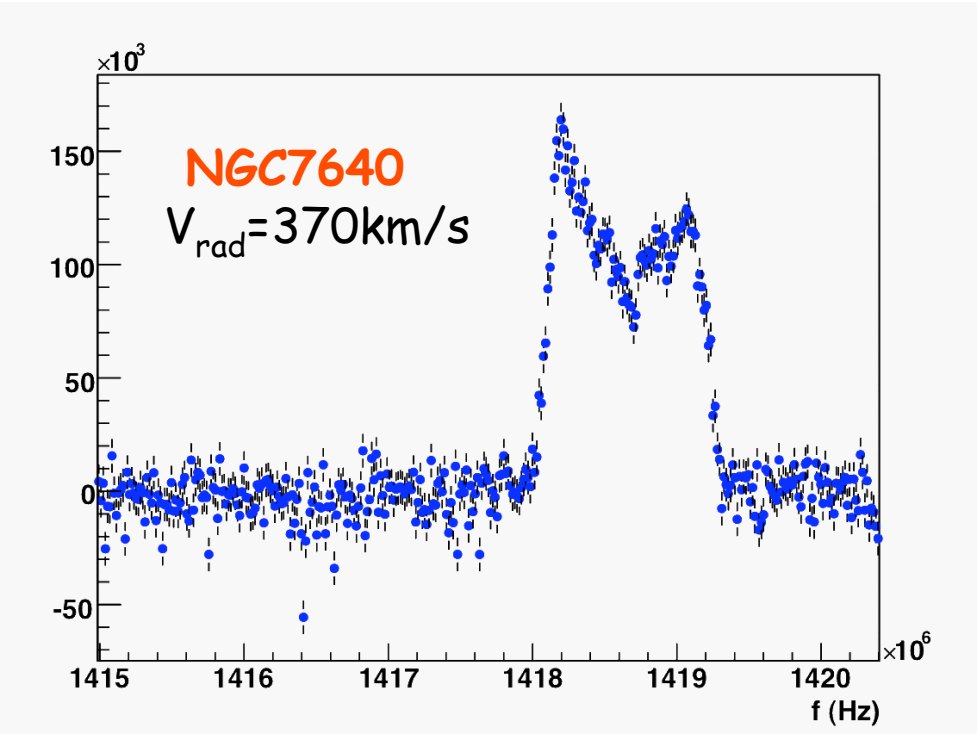
- Equipment of the two RT dipoles with our electronic chain directly in the focal carriage

Three test campaigns:

- **Dec. 2007:** Tests of the analog electronics and clock distribution system
- **Summer 2008:** Tests of the final ADC boards and PCI-express boards (one channel)
- **Spring 2009:**
  - **March 09:** Same as summer tests with several channels and a faster read-out.
  - **April 06:** Same + on-the-fly FFT in FPGA

FFT computed off-line

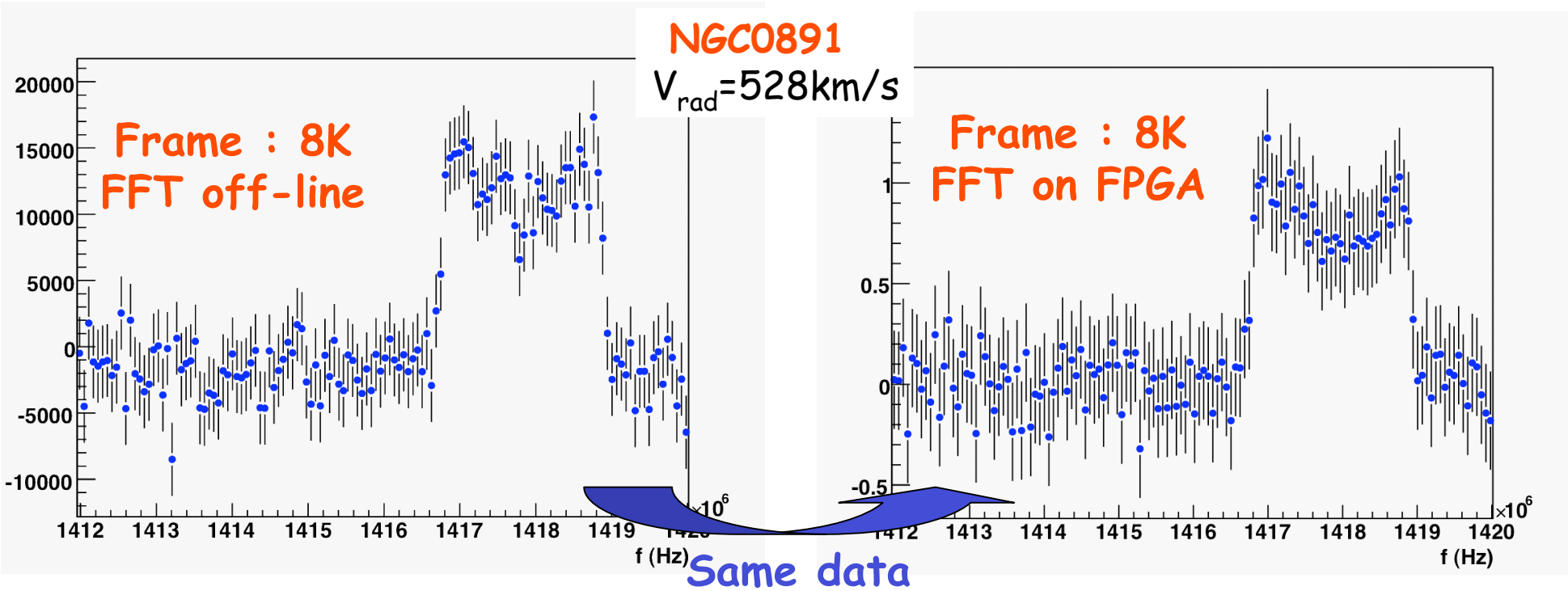




Results:

- 4 channels
- Frame : 32k samples per channel
- Read-out on disk: 2x100 MB/s
- Resolution: (15kHz)

On-the-Fly FFT on FPGA



Tests of the FFT:

- 2 channels (raw data) 2 channels (on-the-fly FFT)
- Frame : 8k samples per channel
- Resolution: (60kHz)
- Comparison for the same data (FFT off-line - FFT on FPGA)
- **Preliminary results very promising!!!**

Test in Pittsburgh with cylinder prototype

Tests in Pittsburgh

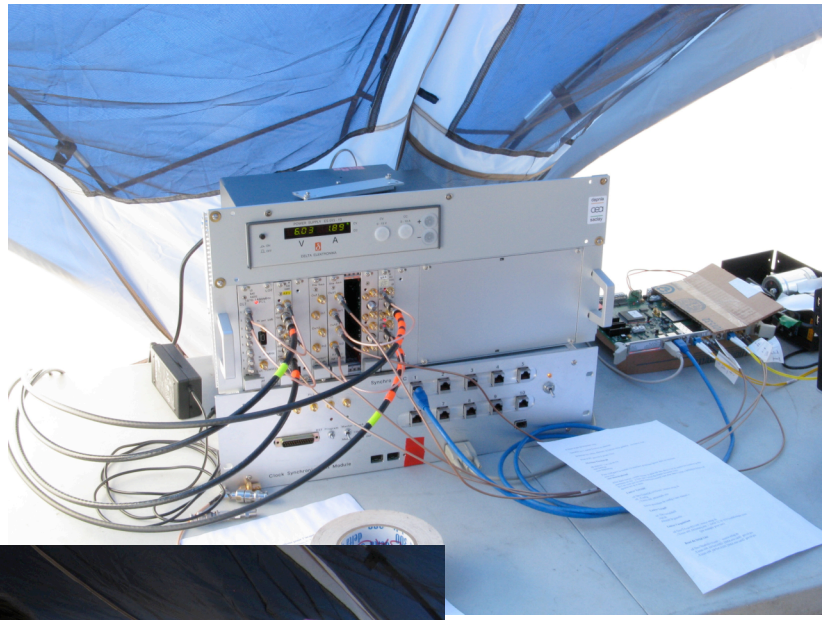
Strategy

- Measurements of the visibility between cylinders ($a_1 a_2^*$)
- Tests different firmware (with simple sampling and with FFT on board FPGA)
- Compare with or without downconversion.

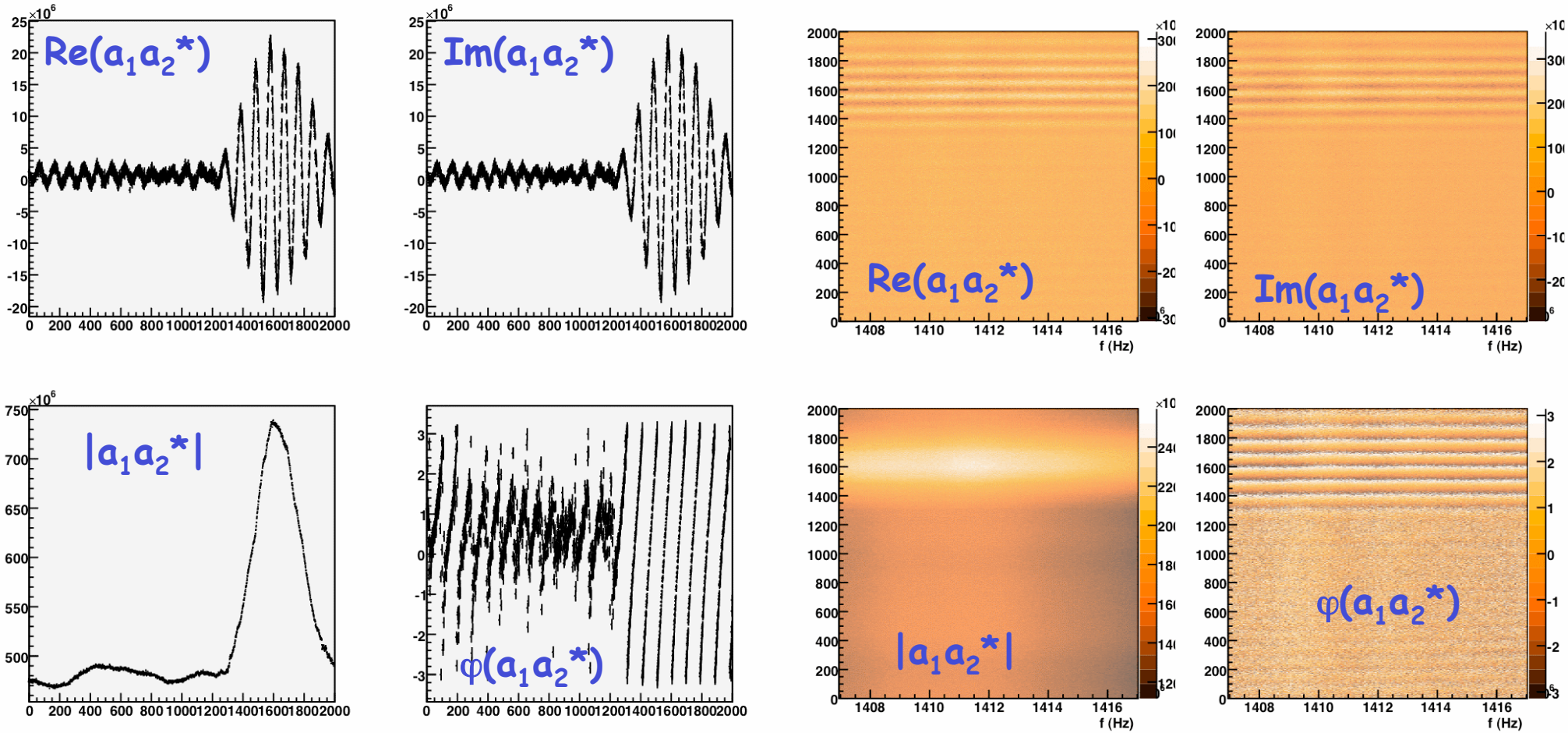
Several test campaigns foreseen:

- **June 2009:** Correlations between 2 cylinders (4 channels)
- **Fall 2009:** North-South beam forming (16 channels)
- **Spring 2010:** 32 channels with FPGA correlators

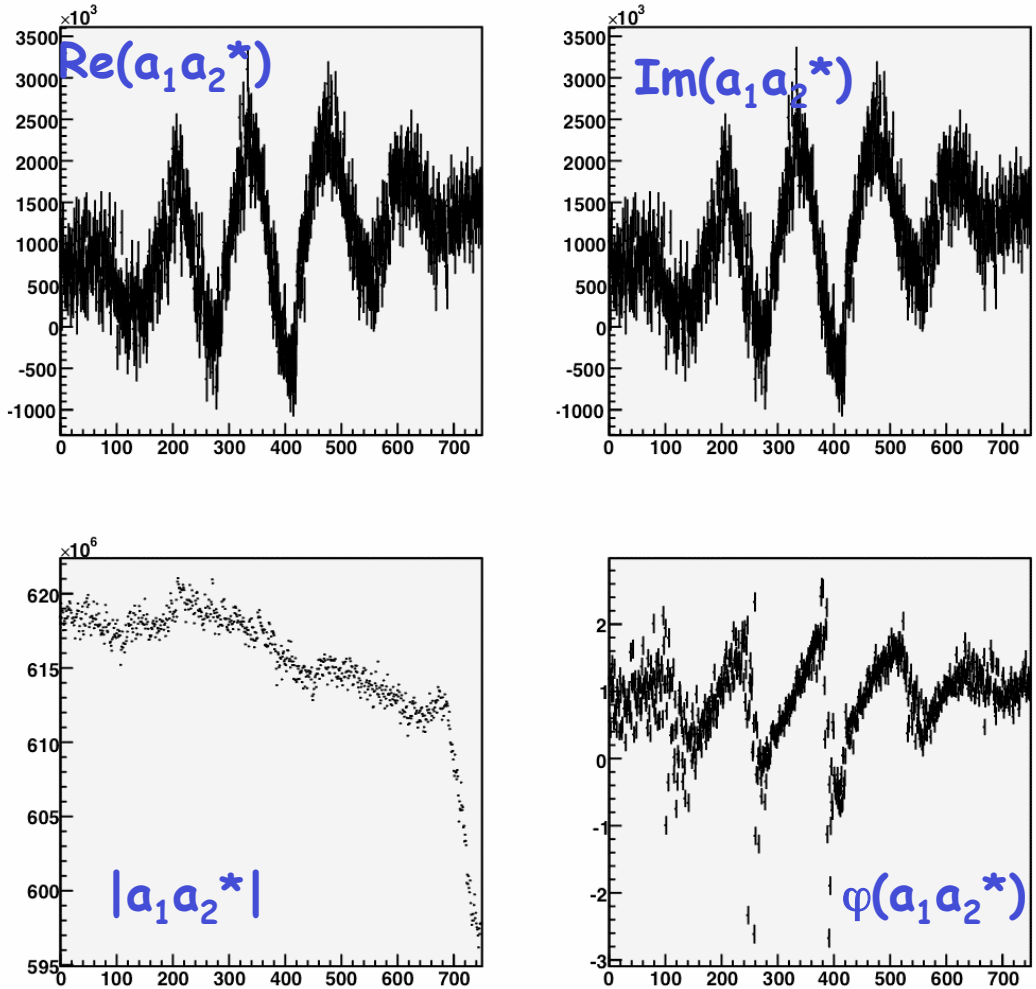
Electronics set up in Pittsburgh



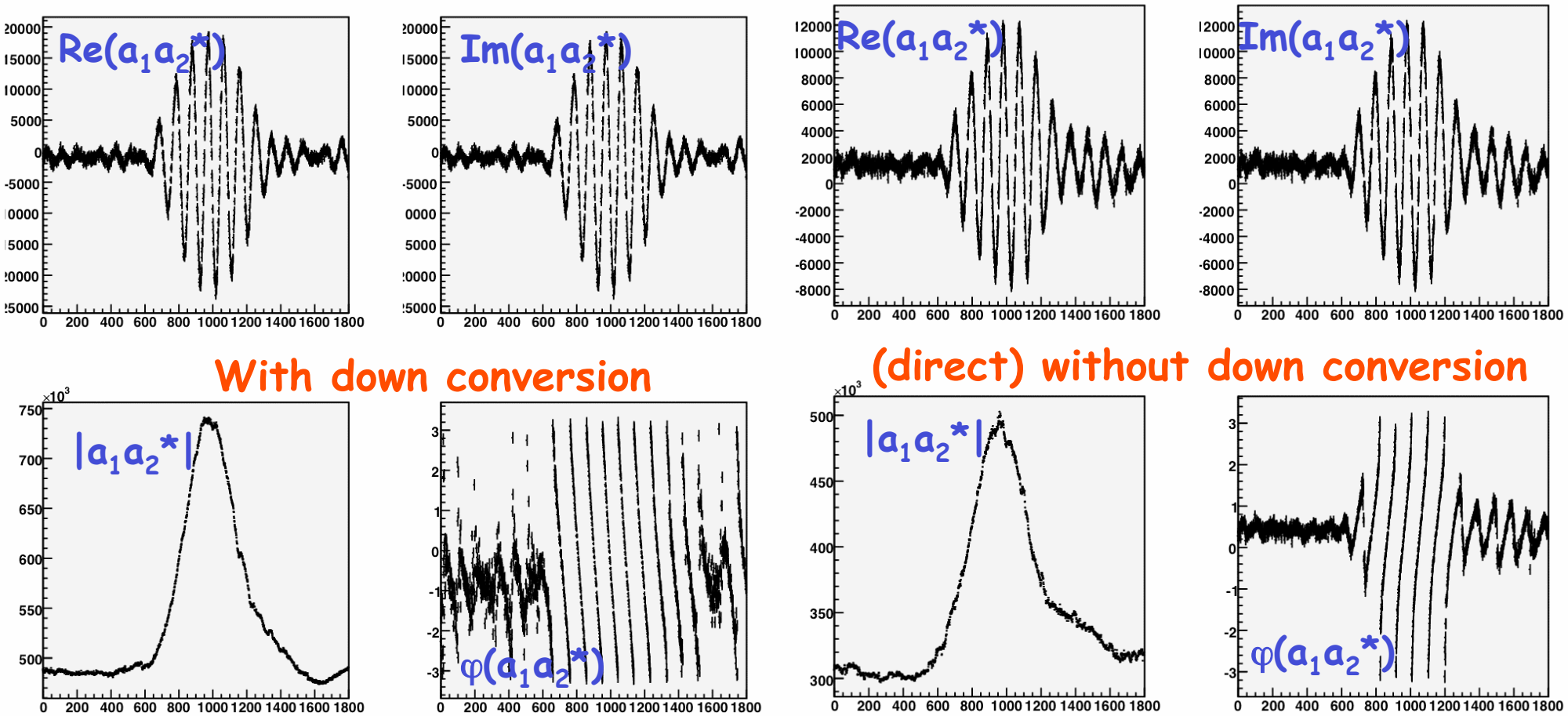
Sun Transit with "down conversion"



Cas-A Transit



Sun Transit with on-the-fly FFT



Conclusions

Conclusions

- The time resolution (jitter) is better than 10 ps
- In under-sampling mode the resolution is also at 10ps
- Promising tests with the FFT on FPGA but few problems are still to be fixed!
- Very encouraging first results in Pittsburgh with the visibility measurements