
CRT ELECTRONICS

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- * Based on the development work done jointly in France by IRFU (CEA , Saclay) and LAL-IN2P3 (CNRS, Univ. Paris Sud, Orsay) for 21cm BAORadio/CRT project since 2006
- * Physicists : C. Magneville, C. Yèche, R. Ansari
- * Engineering team: P. Abbon, C. Beigbeder, D. Breton, D. Charlet, E. Delagnes, H. Deschamps, P. Kestener, B. Mansoux, C. Pailler, M. Taurigna

See C.Yèche's presentation

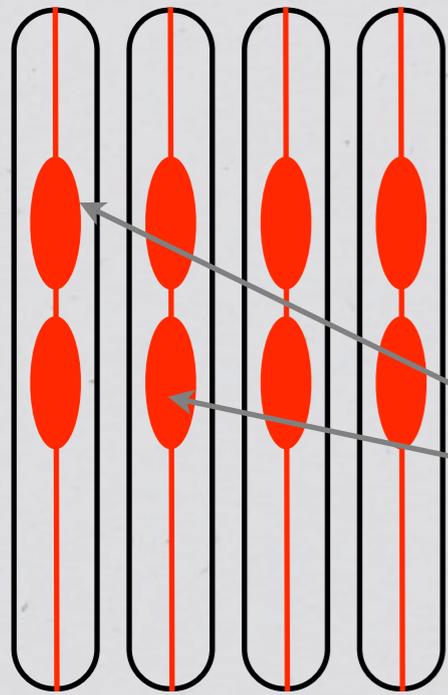
Some figures

- * 500 receivers (analog) / cylinder / polarisation
- * 5000 analog channels / polarisation
- * 1000 digital channels / polarisation after analog sum ?
- * RF frequency band : 650-900 MHz ($z = 0.5 \dots 1.1$)
- * Total data rate : 500 GBytes/sec ... 1 TBytes/sec

CRT electronic components

- * AS1 : Analog Stage 1
- * AEM : Analog Electronic Module
- * DIG / TFFT : Digitizer, or Digitizer + Time FFT (or PFB)
- * FGRP / BFORM : Data grouping per frequency / Along the cylinder beam forming
- * **DCLK : Clock/control signal Distribution**
- * **CORCYL : Visibility computation**

Option I



ASI : Analog Stage I

AEM

DIG

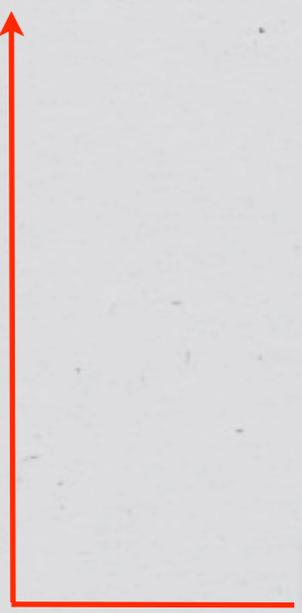
Optical link /
Ethernet



APCCL

Acquisition and Processing
Computer Cluster

DCLK



AS1 : First stage analog module

- * AS1 is located in the focal plane / CRT focal line
- * Antenna / LNA / filters board design
- * Do we use LO on the antenna board ?
- * RF summing stage : number of receivers summed, possibility of inserting delays/phase ... ?

Questions :

- * What is the electronic (amplifier noise) we can reach (5-10 K ?) and what would be the system temperature ? Can we gain a factor 2 in system temperature (50 K -> 25 K ??)
- * What is the “minimum” number of channels through RF summing ?
- * LO or undersampling, how do we replace LO phase modulation, can we make the filters good enough. LO good if we want to send the signal over long distance.
- * LO would make the system frequency agile
- * Can we trade bandwidth (250 MHz -> 50 MHz) against sampling all receivers ?
- * If we have the gain in system temperature, (factor 2), we reach the same sensitivity in 1/4 of the time -> 4 x 50 MHz survey in a year

AEM / DIG

The **AEM** (Analog Electronic Module) and the Digitization system **DIG** is located near the telescope

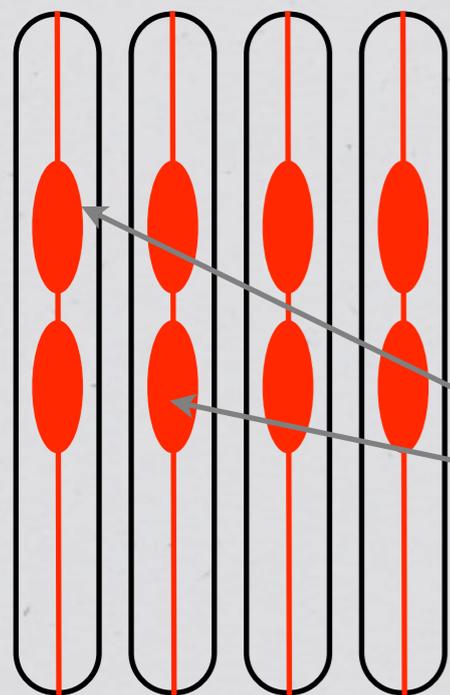
AEM : Analog Electronic Module

- * Signal processing at RF (1 GHz) or IF (250 MHz) ?
- * LO at the AEM level , if IF
- * Do we use LO on the antenna board ?
- * RF summing stage : number of receivers summed, possibility of inserting delays/phase ... ?

DIG : Digitization system

- * Digitization : RF (1 GHz) undersampling mode or IF (250 MHz)
- * The bandwidth ?
- * Digital signal transmission mode / media to the next processing stage or the computer cluster

Option 2 : perform decomposition to frequency component on the Digitization board



ASI : Analog Stage I

AEM

DIG

TFFT

Optical link / Ethernet

~ 1000 optical links



APCCL

Acquisition and Processing Computer Cluster

DCLK

DIG / TFFT

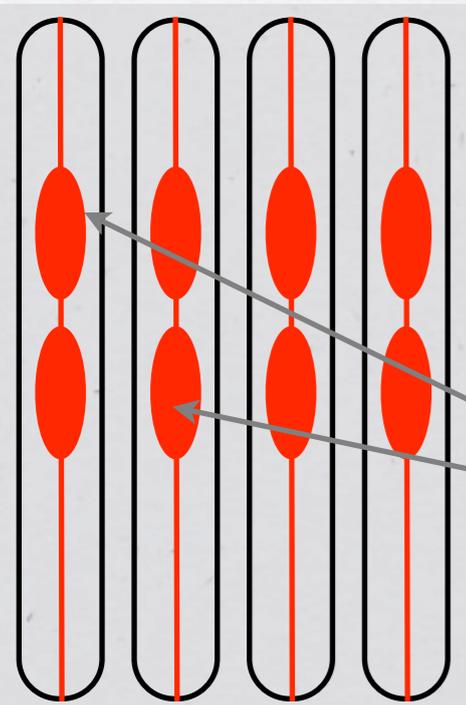
- * Do we perform frequency component separation using FPGA's embedded in the digitization system ?
- * Do we use FFT like algorithm (Time-FFT) or other frequency decomposition methods (PFB ...) ?
- * What would the target frequency resolution be ?

$$z = 1, \delta z = 0.001 \longrightarrow \delta \nu \simeq 350 \text{ kHz}$$
$$\delta z = 0.001 \longrightarrow \delta \ell \sim 5 \text{ Mpc} \ll \ell_{BAO} \sim 150 \text{ Mpc}$$

Beam-Forming, correlations ?

- * CRT will produce a huge 'continuous' data flow: 1000 GBytes/sec (\sim TB / sec) - this is about the total memory bandwidth of 1000 'standard' computers !
- * Should we try to do more processing on dedicated electronic systems ?
- * The data from the TFFT output has to be re-arranged and combined (linear combination) to make the beams along the cylinder

Option 3 : do data rearrangement (beamforming) using dedicated electronics



ASI : Analog Stage I

AEM

DIG

TFFT

BFORM

10 Gbit

Eth

Optical link

~ 1000 optical links



APCCL

Acquisition and Processing Computer Cluster

DCLK



- * Data rearrangement can be done using CPU's and network, but it needs carefully engineered network and it costs memory bandwidth
- * FGRP : Data rearrangement can be done “easily” and at low cost using a modular system using FPGA's and serial links
- * BFORM : Do we want to do beam forming (along the cylinders) on dedicated electronics ?
- * Note that there is no data flow reduction until signal from different cylinders is correlated (or combined)

DCLK : Clock/ control signal distribution

- * DCLK provides synchronous clocks to all digitizations boards, as well as other synchronous control signals (StartOfPaquet...)
- * DCLK can also provide the LO reference signal and the phase modulation control signal
- * Possible solution : use optical fibers and digital streams to distribute synchronous signals from a central facility to the electronic boxes (or crates) located near the cylinders

Electric power

- * Electric power production : use of diesel generators ?
- * Digitization+TFFT < 10 W/Ch (compared to 100 W/CPU core)
- * How do we distribute the power to AS1, AEM, DIG/TFFT ?
- * Cost of the power production and distribution infrastructure
- * Running cost for electricity production production (20 kW / 1000 channels for AEM+DIG/TFFT , 300 kW for 1000 CPU's !)