

Testing of IPAS Latch-TDC

Da-Shung Su

Jia-Ye Chen, Hsi-Hung Yao, Su-Yin Wang,
Ting-Hua Chang, Wen-Chen Chang

2011/07/23

“Latch”-TDC

- Each channel consists of a shift register with a depth of 128 clocks. Whenever there comes a wire chamber signal, a hit is registered. The actual depth of the shift register is determined by the need of trigger latency.
- The signal of one channel will be sampled by the clock with four different phases and be placed in four shift registers respectively.
- The hit pattern sampled by four PLLs is represented by **4 bits** for each channel, as shown in the table.
- Upon the arrival of a trigger, the hit pattern of an accepted window of 64(32)-step width in the shift register, **$64(32)*4=256(128)$ bits= $32(16)$ bytes**, will be copied to the output memory for each channel. This CIP action introduces the dead time of TDC module.
- **The timing information could be retrieved from the "position" of the hit in the shift register and the preset delay time. Multi-hit information is also preserved.**

Current Design Specification

	Station 1
Time bin	10 ns
Width of accepted window	32*10=320 ns 64*10=364 ns
Maximum Delay of shift register	128*10=1,280 ns (>1,100 ns)
Time resolution of TDC	2.5 ns
Two-hit resolution	10 ns

Frequency of clock source: 100 MHz

TDC firmware: <http://dl.dropbox.com/u/1025275/83591130.pdb>

VME hardware: Version 2.2, 135 MHz clock setting.

Sampling Results and Output

- At each time bin, Q0, Q1, Q2 and Q3 are the sampling results of the input signal with the four different phases of the clock.
- Q0 is the starting phase, i.e. $t(Q0)$ is earlier those of the others.
- “x” stands for either 0 or 1.
- We assume that two hits are separated from each other more than 1 clock away, and a valid hit sustains more than 1-clock wide.

Sampling Results				for Output			
Q3	Q2	Q1	Q0	Y2	Y1	Y0	
0	0	0	0	0	0	0	0 → No signal
X	X	1	0	0	0	1	1 } 2 } 3 } Leading edge detected.
X	1	0	0	0	1	0	
1	0	0	0	0	1	1	
1	1	1	1	1	0	0	4 → Signal on.
X	X	0	1	1	0	1	5 } 6 } 7 } Trailing edge detected.
X	0	1	1	1	1	0	
0	1	1	1	1	1	1	

VME Address Map

Offset	Access	Data width	Description
0x000	R/W	D32	Control and Status Register (CSR)
0x004	R	D32	PCB serial number and Revision date code
0x008	R	D32	FIFO status register
0x00C	R/W	D32	Control and Status Register (CSR2)
0x010	W	D32	FIFO test mode enable
0x014	W	D32	FIFO test mode disable
0x020	W	D32	Clear
0x028	W	D32	Latch mode enable
0x02C	W	D32	Latch mode disable
0x050	W	D32	Reserved
0x054	W	D32	Reserved
0x060	W	D32	Reset
0x068	W	D32	Generate output pulse
0x100 0x1FC	R/W, BLT	D32	128KB FIFO memory space, (32K x 32)

CSR2 0x0c (32 bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Spare			Delay Time (Write)					Spare							64/32 bins	

Data Structure for One Time Bin (10 ns)

1st 32-bit data

D31	D30	D29	D28	D27	D26	D25	D24	...	D7	D6	D5	D4	D3	D2	D1	D0
X	Ch7 Y2	Ch7 Y1	Ch7 Y0	X	Ch6 Y2	Ch6 Y1	Ch6 Y0	...	X	Ch1 Y2	Ch1 Y1	Ch1 Y0	X	Ch0 Y2	Ch0 Y1	Ch0 Y0

2nd 32-bit data

D31	D30	D29	D28	D27	D26	D25	D24	...	D7	D6	D5	D4	D3	D2	D1	D0
X	Ch15 Y2	Ch15 Y1	Ch15 Y0	X	Ch14 Y2	Ch14 Y1	Ch14 Y0	...	X	Ch9 Y2	Ch9 Y1	Ch9 Y0	X	Ch8 Y2	Ch8 Y1	Ch8 Y0

⋮

7th 32-bit data

D31	D30	D29	D28	D27	D26	D25	D24	...	D7	D6	D5	D4	D3	D2	D1	D0
X	Ch55 Y2	Ch55 Y1	Ch55 Y0	X	Ch54 Y2	Ch54 Y1	Ch54 Y0	...	X	Ch49 Y2	Ch49 Y1	Ch49 Y0	X	Ch48 Y2	Ch48 Y1	Ch48 Y0

8th 32-bit data

D31	D30	D29	D28	D27	D26	D25	D24	...	D7	D6	D5	D4	D3	D2	D1	D0
X	Ch63 Y2	Ch63 Y1	Ch63 Y0	X	Ch62 Y2	Ch62 Y1	Ch62 Y0	...	X	Ch57 Y2	Ch57 Y1	Ch57 Y0	X	Ch56 Y2	Ch56 Y1	Ch56 Y0

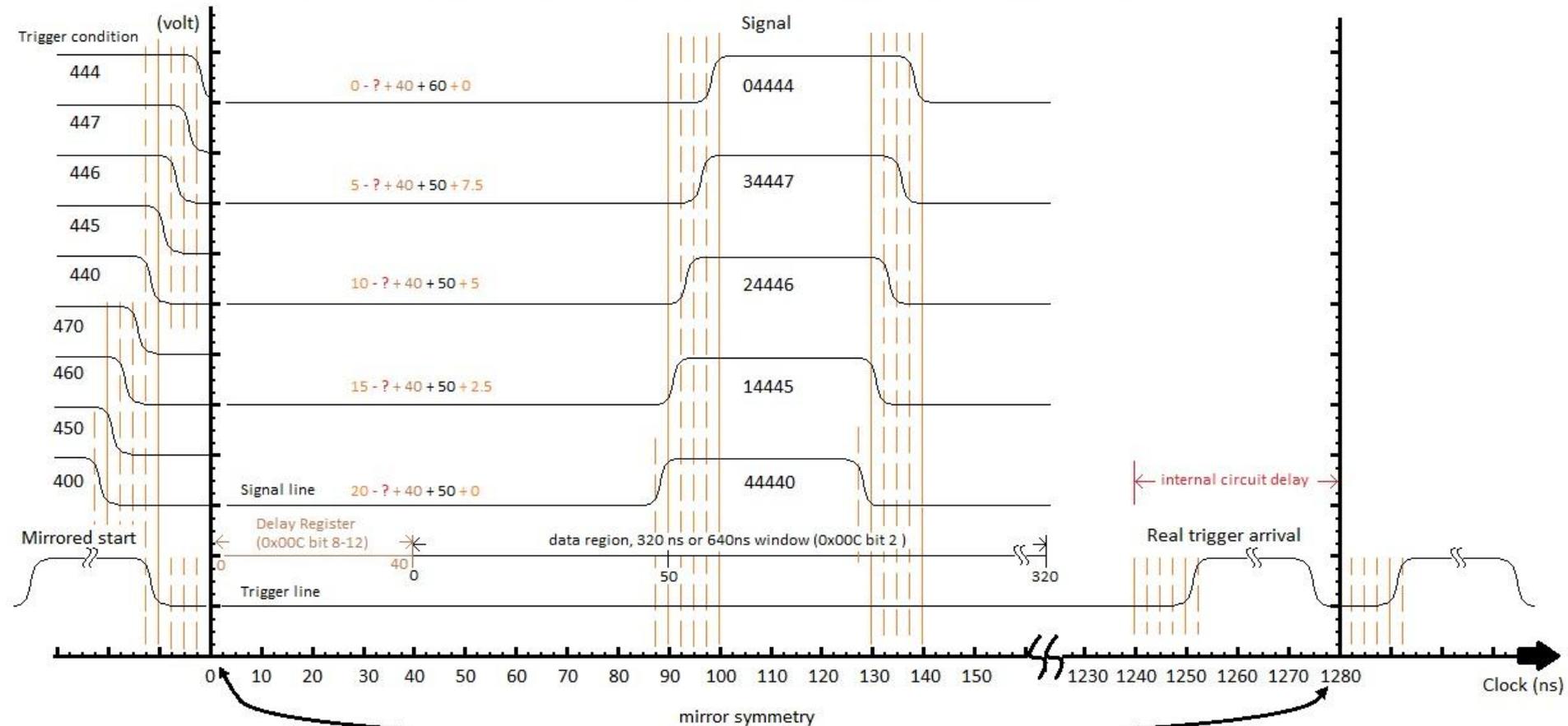
Overall Data Structure for ONE EVENT



Timing Diagram

TDC = Output Window Start
 + Clock of Signal Edge in the Output Window
 + Trigger Correction + Edge Correction
 - Circuit Delay

Formula : fine trigger correction - circuit delay + register delay + clock of rising edge of signal + fine signal correction



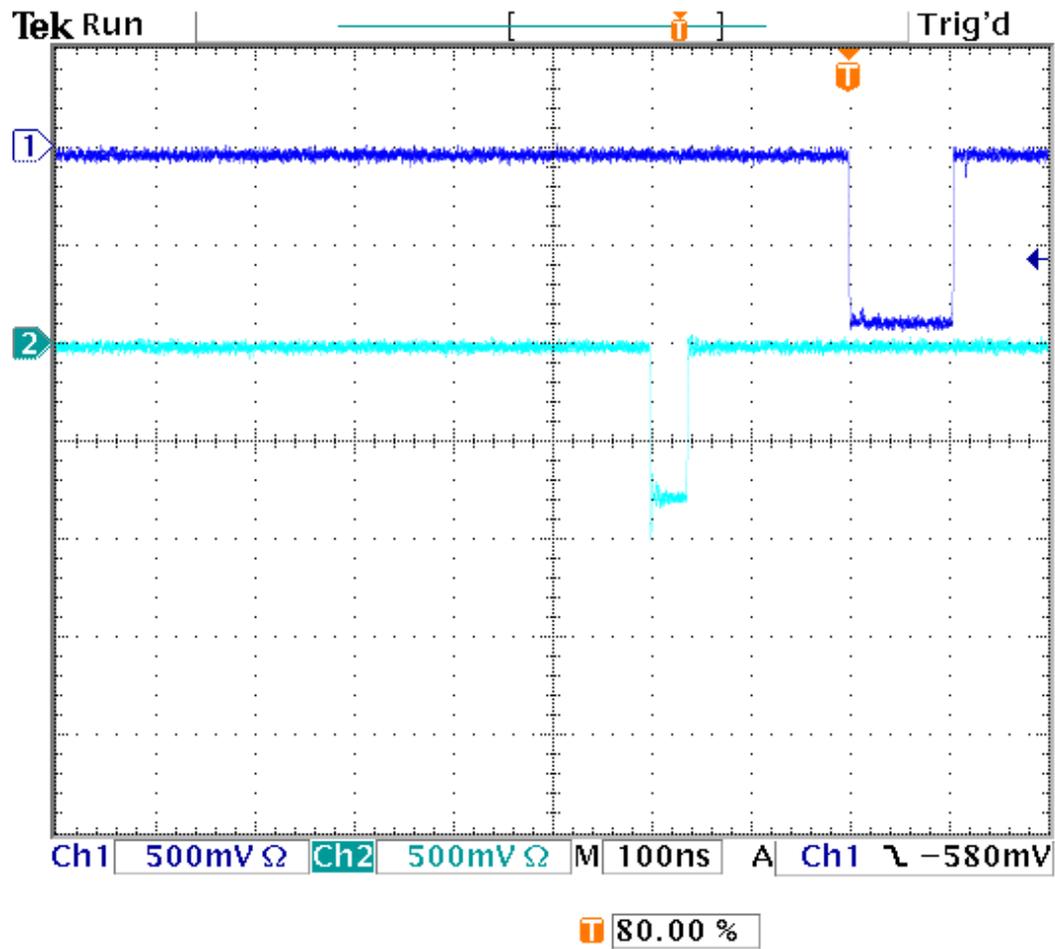
Items to be tested

- TDC resolution (DONE)
- Double-hit resolution (DONE)
- Output window scanning (DONE)
- X-talk (DONE)
- Stability of data for large statistics with the operation of CODA DAQ
 - Single hit with fast regular trigger
 - Random hit

Dead Time for ONE Single Module

- TDC internal data conversion (copy in progress- CIP)
 - 32 time bin: <9.8 us
 - 64 time bin: <17.5 us
- CODA read out dead time (DMA readout)
 - 32 time bin: <95 us
 - 64 time bin: <195 us

Single Hit



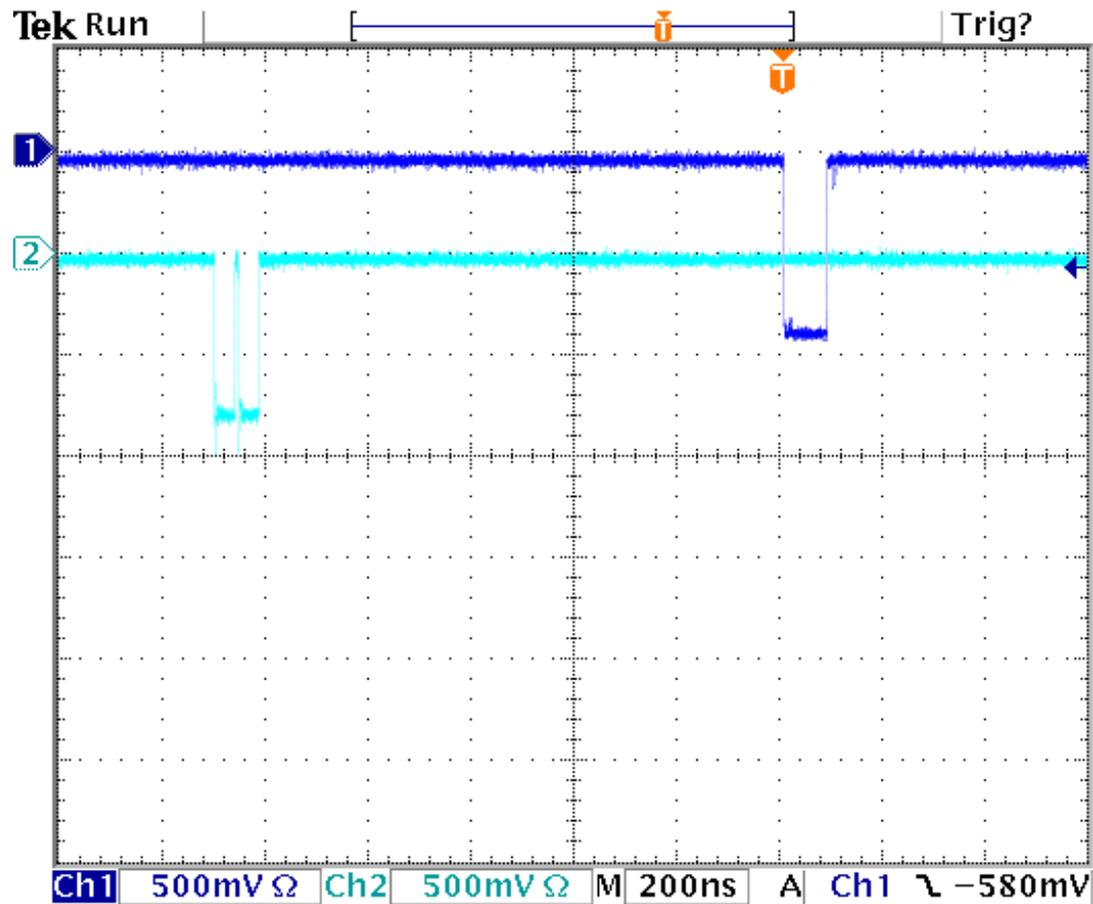
Resolution

Determined by the Scope and TDC

Real time	TDC0	sig corr	trig corr	TDC	Diff	Jitter
194.16	230	7.5	5	242.5	48.34	-1.36
192.92	230	7.5	5	242.5	49.58	-0.12
191.54	230	7.5	5	242.5	50.96	1.26
178.08	220	7.5	2.5	230	51.92	2.22
194.54	220	5	17.5	242.5	47.96	-1.74
181.96	220	5	5	230	48.04	-1.66
174.14	200	5	17.5	222.5	48.36	-1.34
186.28	220	5	10	235	48.72	-0.98
193.18	230	5	7.5	242.5	49.32	-0.38
192.80	220	5	17.5	242.5	49.70	0.00
167.68	200	5	12.5	217.5	49.82	0.12
176.70	210	5	12.5	227.5	50.80	1.10
192.82	240	2.5	0	242.5	49.68	-0.02
192.76	230	2.5	10	242.5	49.74	0.04
169.42	210	2.5	7.5	220	50.58	0.88
191.84	240	2.5	0	242.5	50.66	0.96
191.48	220	2.5	20	242.5	51.02	1.32
188.36	230	0	7.5	237.5	49.14	-0.56
170.46	200	0	20	220	49.54	-0.16
174.92	210	0	15	225	50.08	0.38
					49.70	

- Input a single pulse. The time of leading-edge w.r.t. the trigger is measured by the oscilloscope – “Real time”.
- $TDC = [TDC0] + [sig\ corr] + [trig\ corr]$
 - TDC0: position of leading edge
 - Signal correction: fine correction of leading edge of signal by 4-phase sampling.
 - Trigger correction: fine correction of leading edge of trigger by 4-phase sampling.
- There is a common difference between “Real time” and “TDC”, in average of 49.70, possible caused by the cable and electronics modules.
- The jitter relative to the common difference is within **2.5 ns**.

Double Hits



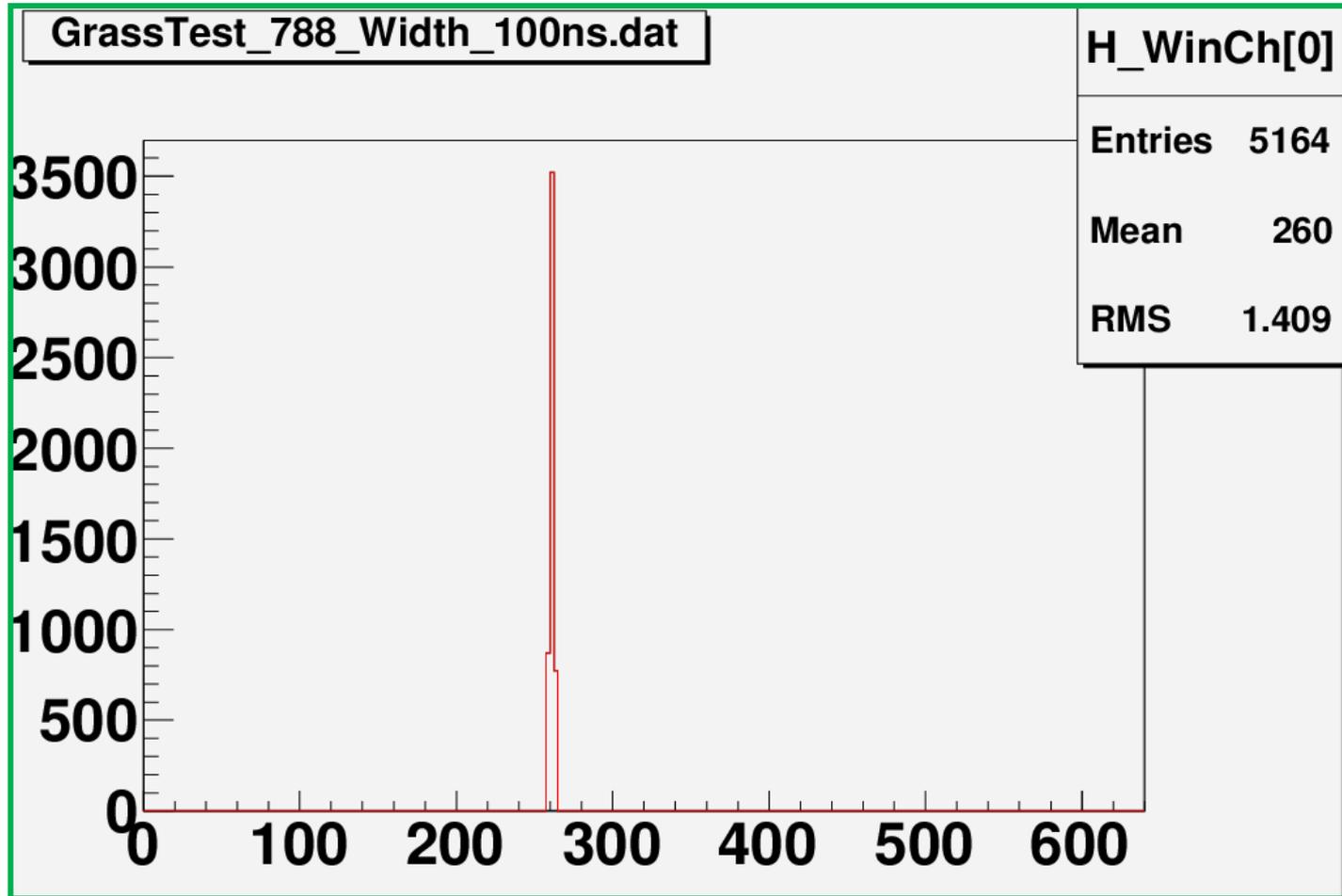
70.60 %

12 Jul 2011
03:33:06

Double-Hit Time Structure Measured by the Scope and TDC

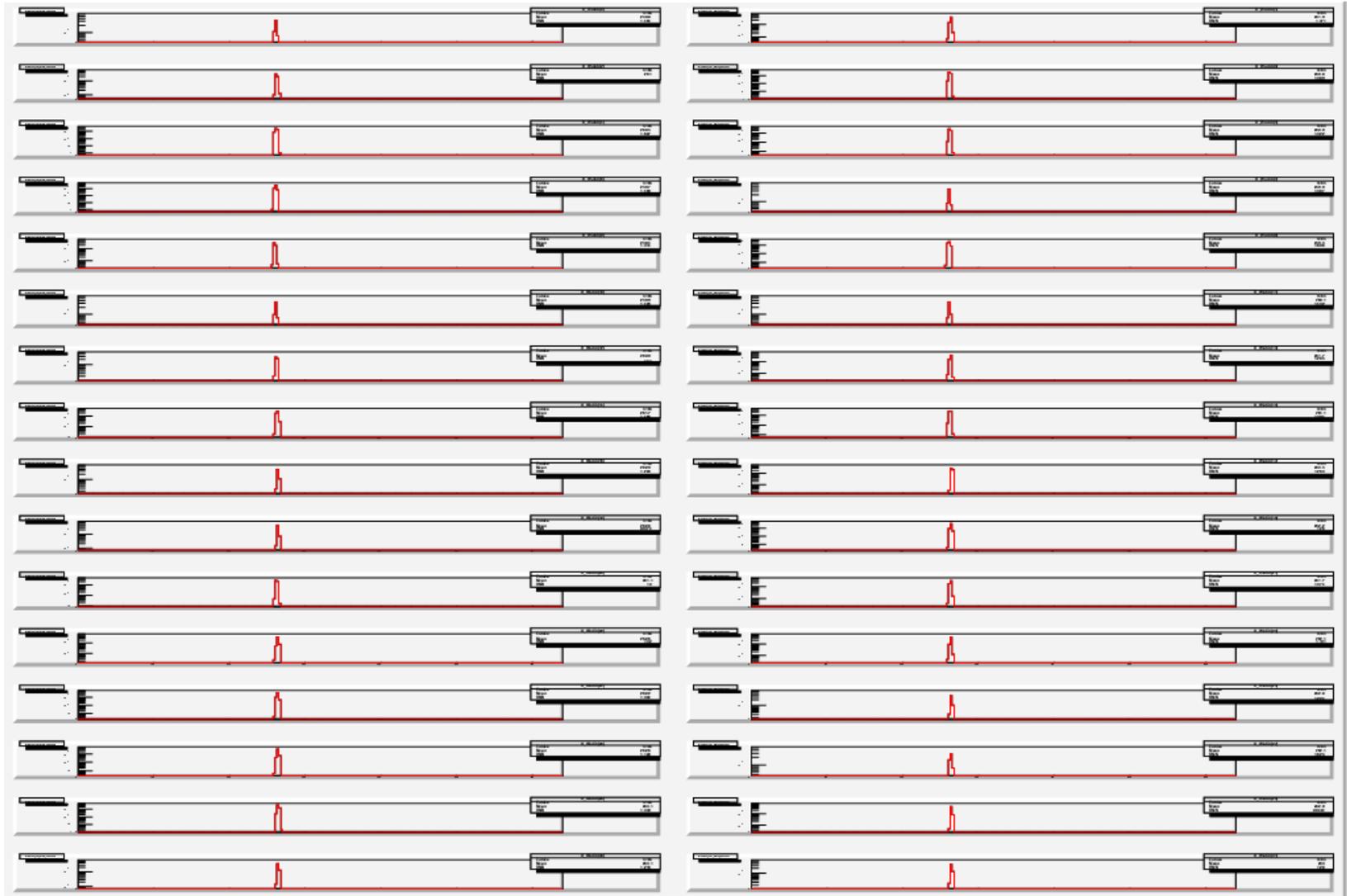
1-64	start clock1	start clock 2	TDC value1	TDC value2	signal 1 Fall Edge	signal 1 Rise Edge	signal 2 Fall Edge	R-F			Error of Sig1	Error of Sig2
3	7	444434446	34446	1295.06	1255.40	1247.78	7.62	7.50	0.12	0.26	-1.01	
6	10	444424446	24446	1274.80	1235.24	1229.80	5.44	5.00	0.44	0.00	-1.49	
5	9	244464447	64447	1265.96	1226.60	1221.68	4.92	5.00	-0.08	-1.34	2.89	
5	9	244454447	54447	1268.64	1229.10	1223.66	5.44	7.50	-2.06	1.34	2.37	
6	10	244454447	54447	1267.38	1227.82	1223.16	4.66	7.50	-2.84	0.08	1.87	
4	8	244454447	54447	1276.80	1237.12	1232.04	5.08	7.50	-2.42	-0.50	0.75	
6	10	244454447	54447	1268.08	1228.58	1223.28	5.30	7.50	-2.2	0.78	1.99	
5	9	144454447	54447	1267.08	1227.52	1221.92	5.60	7.50	-1.9	-0.22	3.13	
4	8	144454447	54447	1283.40	1243.84	1237.06	6.78	7.50	-0.72	-1.40	0.77	
6	10	144434446	34446	1274.42	1234.82	1229.20	5.62	7.50	-1.88	2.12	0.41	
7	11	144434446	34446	1267.00	1227.46	1222.72	4.74	7.50	-2.76	-0.30	-1.07	
4	9	34447	14445	1271.80	1232.16	1227.08	5.08	5.00	0.08	-0.50	-1.71	
5	10	34447	14445	1269.84	1230.34	1225.46	4.88	5.00	-0.12	0.04	-0.83	
5	10	34447	14445	1271.92	1232.36	1227.20	5.16	5.00	0.16	-0.38	-1.59	
5	10	34446	1444	1265.52	1226.06	1221.14	4.92	7.50	-2.58	0.72	-0.15	
6	11	34446	14445	1270.86	1231.36	1225.86	5.50	7.50	-2	1.06	-0.43	
3	8	34446	24445	1285.68	1246.00	1239.04	6.96	10.00	-3.04	0.88	0.25	
5	10	34446	1444	1272.98	1233.42	1228.50	4.92	7.50	-2.58	-1.82	-2.79	
3	8	24445	1444	1294.72	1255.12	1247.48	7.64	10.00	-2.36	-0.08	-1.31	
3	8	24445	1444	1294.12	1254.50	1246.76	7.74	10.00	-2.26	-0.68	-2.03	
					1233.95	1228.39					準!	

Arrival Time of a Single-Hit Input (Large statistics recorded by CODA)

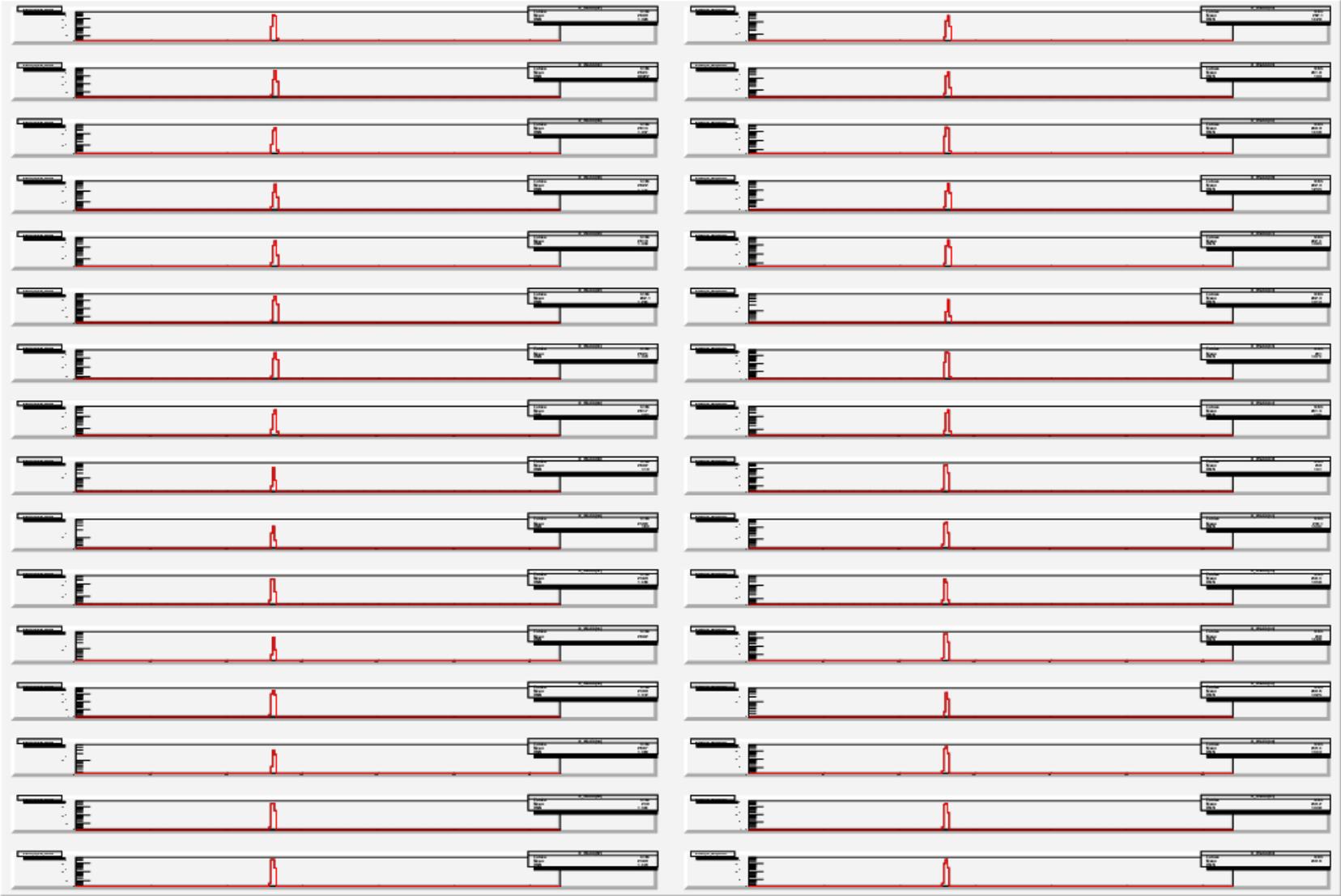


Measured time of leading edge of hits(ns)

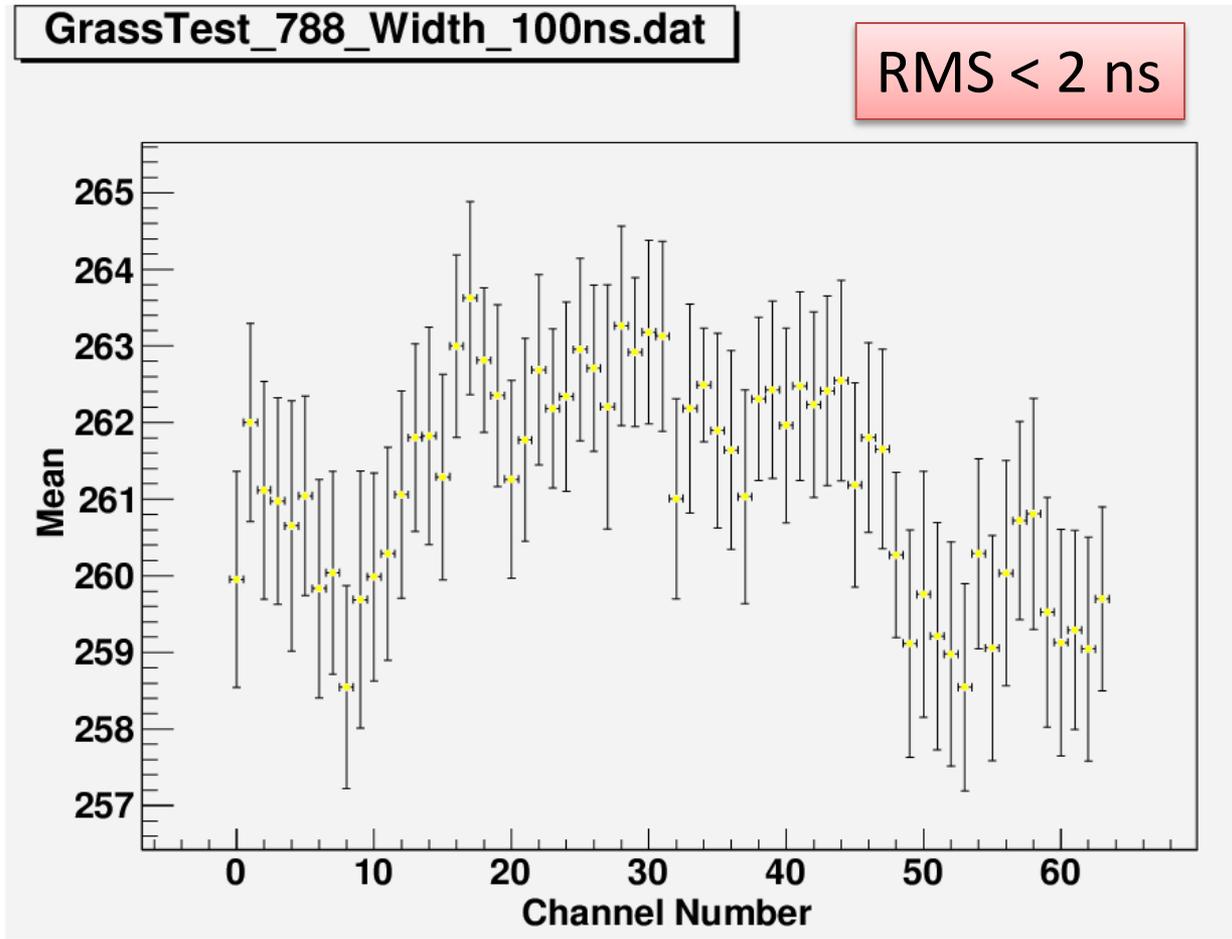
Global View of Channel 0-31 (log scale)



Global View of channel 32-63 (log scale)

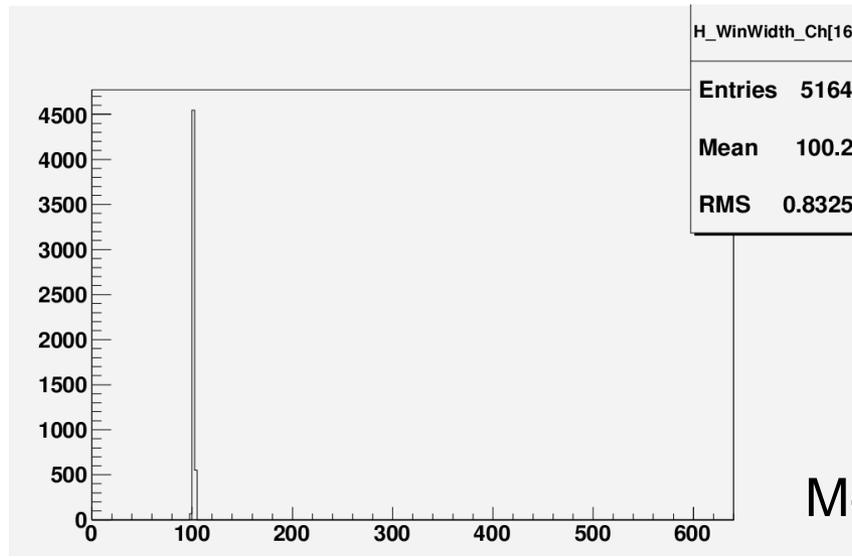


Mean and RMS of Arrival Time of a Single-Hit Input



Channel-dependent mean is caused by the cable and electronics of input signal.

Single Pulses with Fixed Width: Studying TDC NON-linearity

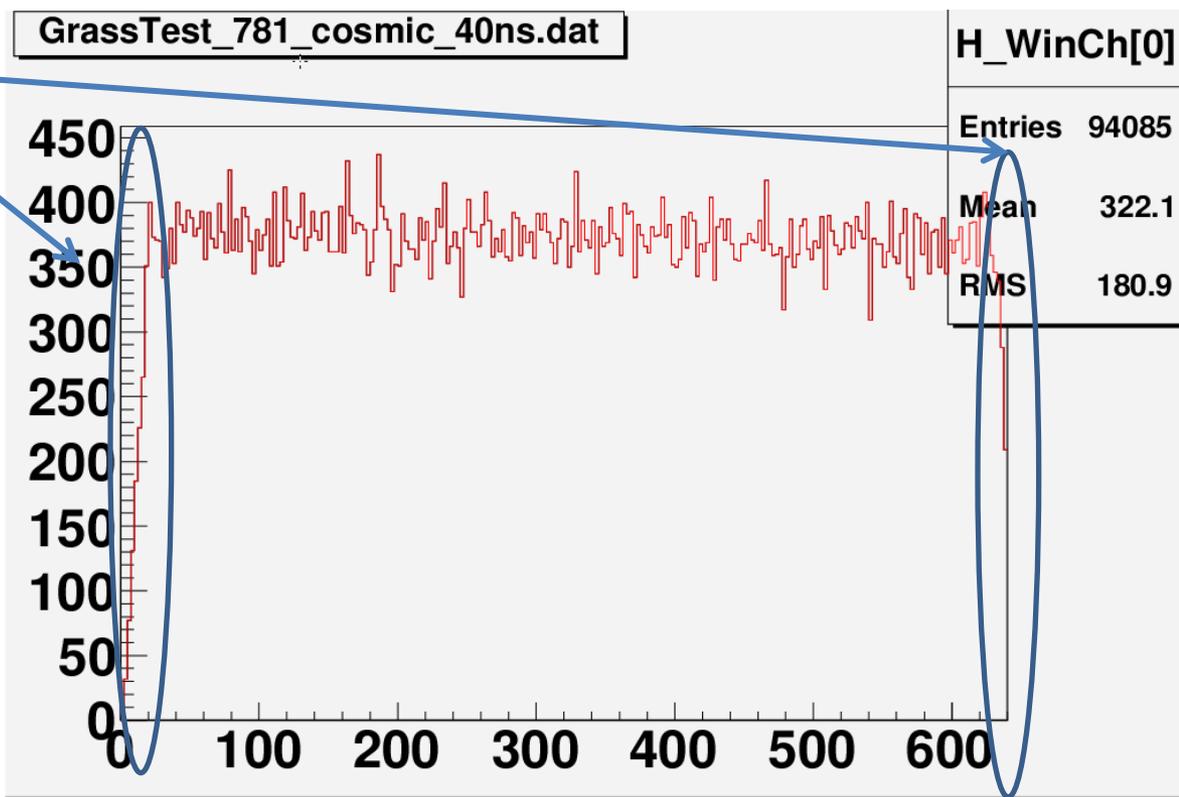


Measured width of input pulses(ns)

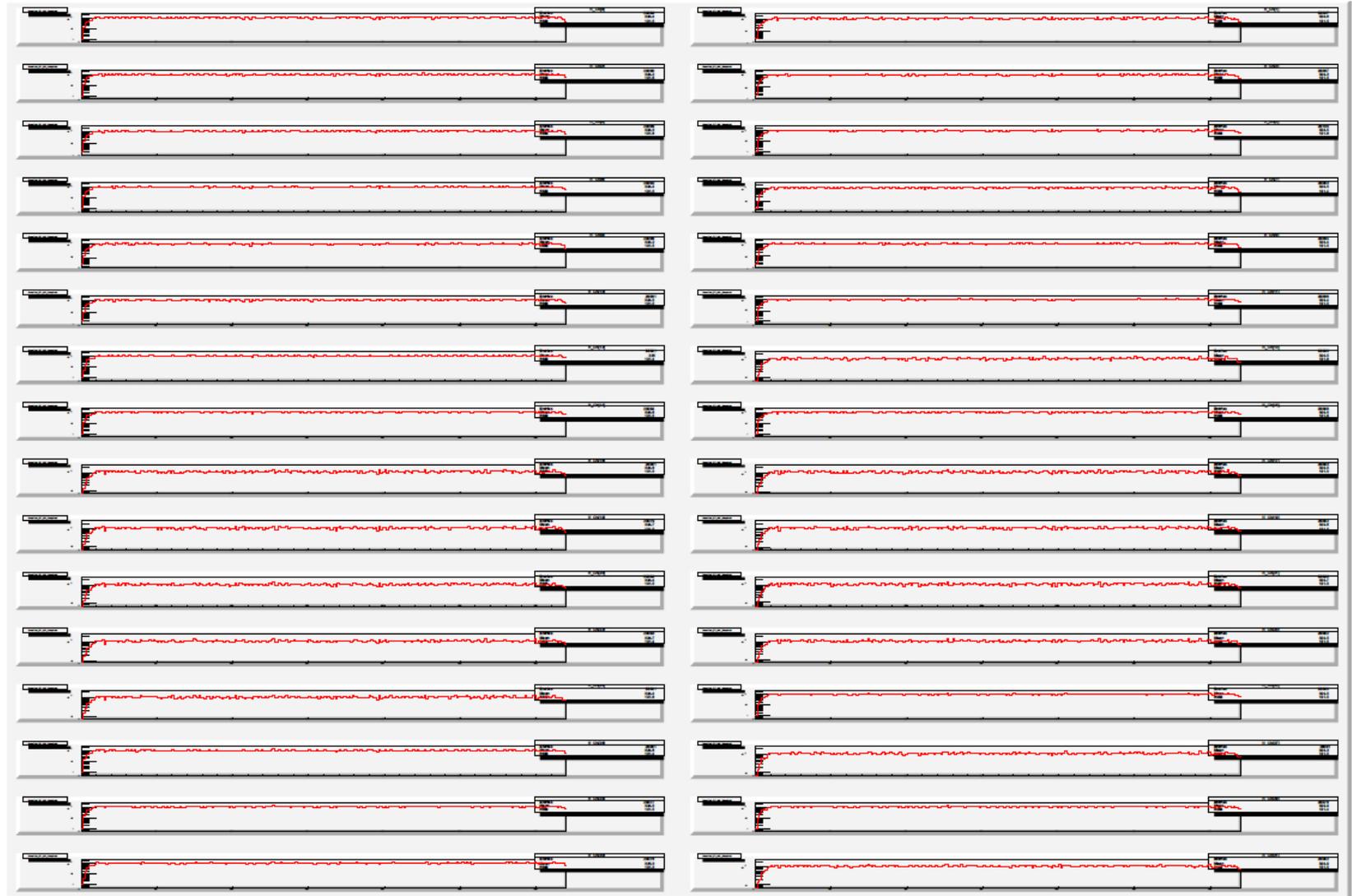
Input Width			Measured Width	
Averaged (ns)	Max (ns)	Min (ns)	Mean (ns)	RMS (ns)
100.218	102.1	98.6	100.2	0.8325
200.0	201.1	199.1	200.1	0.7691
300.413	302.1	299.6	299.6	1.039
399.853	401.1	398.1	399.7	1.056
499.583	501.6	498.1	499.7	1.099

Random Hits

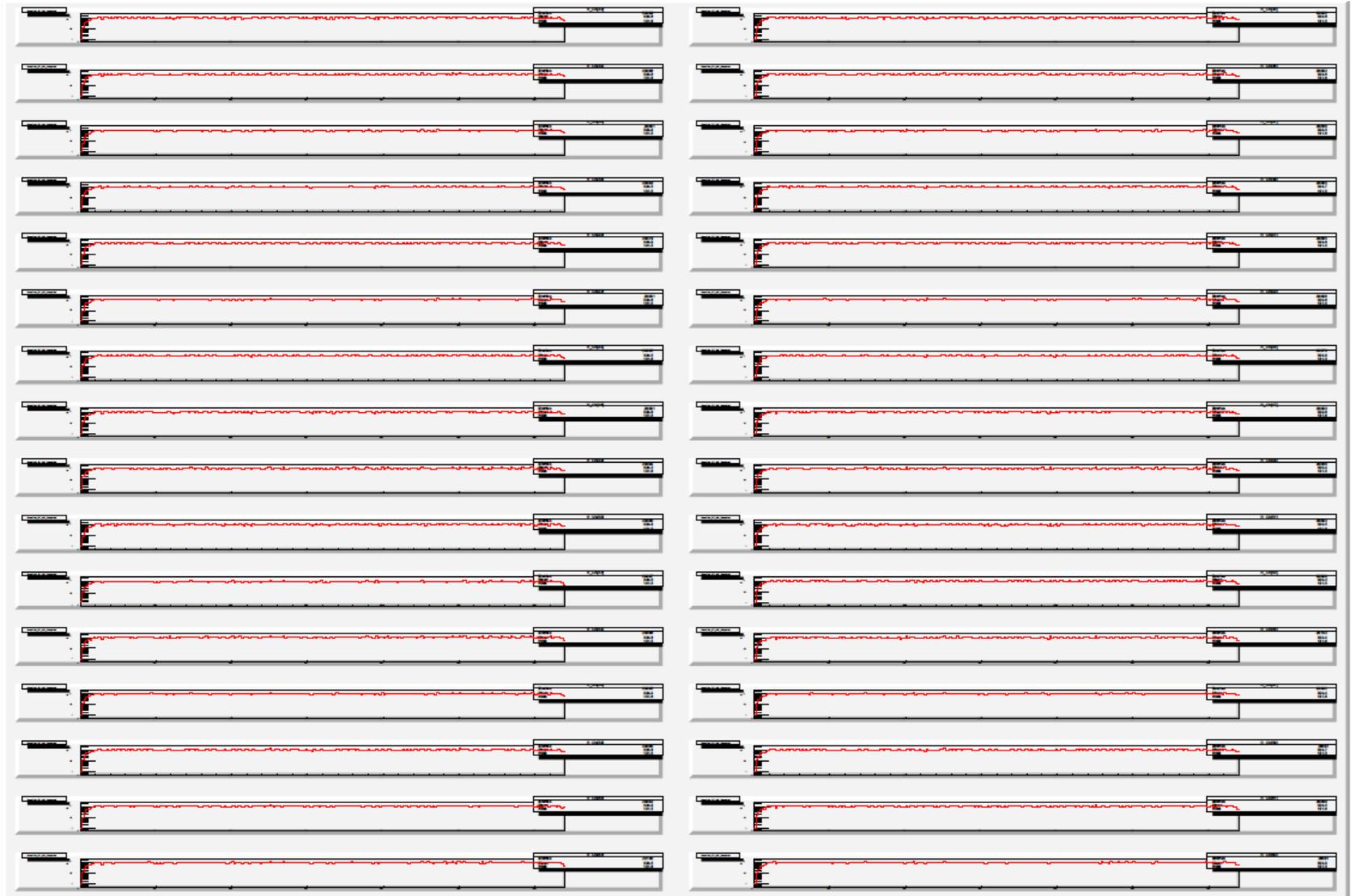
- Output window scanning
- Bin size=2.5 ns
- Signal on the edge of accepted window with ambiguity in the time value are removed.



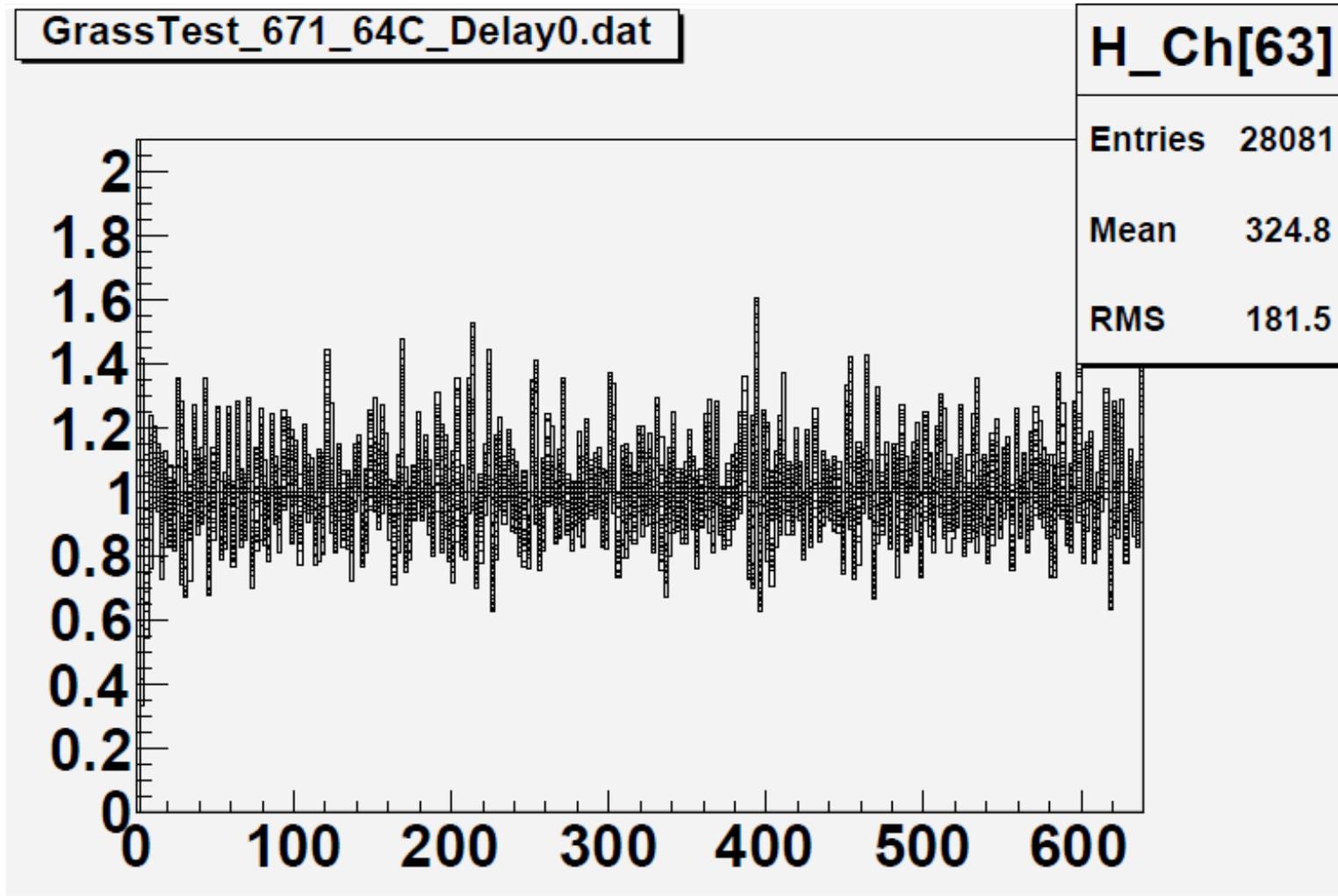
Global View of Channel 0-31 (log scale)



Global View of Channel 32-63 (log scale)



Ratio of Timing Distribution of Random Hit of Channel 0-63 and Channel 0



Cross-talk Checkup

TEST 2

TEST 1

- All odd channels on, even channels off,
- All even channels on, odd channels off
- No sign of X-talk for 50,000 events.

Channels with signal input				Number of events safe from X-talk
Ch1	Ch17	Ch33	Ch49	10,000 events
Ch2	Ch18	Ch34	Ch50	10,000 events
Ch3	Ch19	Ch35	Ch51	10,000 events
Ch4	Ch20	Ch36	Ch52	10,000 events
Ch5	Ch21	Ch37	Ch53	10,000 events
Ch6	Ch22	Ch38	Ch54	10,000 events
Ch7	Ch23	Ch39	Ch55	10,000 events
Ch8	Ch24	Ch40	Ch56	10,000 events
Ch9	Ch25	Ch41	Ch57	10,000 events
Ch10	Ch26	Ch42	Ch58	10,000 events
Ch11	Ch27	Ch43	Ch59	10,000 events
Ch12	Ch28	Ch44	Ch60	10,000 events
Ch13	Ch29	Ch45	Ch61	10,000 events
Ch14	Ch30	Ch46	Ch62	10,000 events
Ch15	Ch31	Ch47	Ch63	10,000 events
Ch16	Ch32	Ch48	CH64	10,000 events

QC Test for all TDC Cards

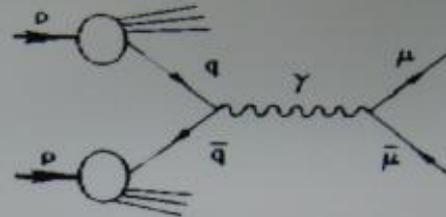
- Stability of data for large statistics with the operation of CODA DAQ
 - Single hit of fixed timing
 - Width=40ns
 - 50,000 events
 - Random hit
 - Width=40ns
 - 80,000 events
- 60 pieces of TDCs were tested and the results are stored at
http://www.phys.sinica.edu.tw/~e906/WWW_public/E906_CR_VME/TDC/production_record/ .

Tag

中央研究院物理研究所

Institute of Physics, Academia Sinica

E906 Experiment
at Fermilab



VME LATCH/TDC
-Production Model
-Version 2.2

+5V/-12V

PCB: 15027-TT1-8359

1045

PM1107A

1107

90

83591-130

July 2011

MADE IN TAIWAN

www.phys.sinica.edu.tw