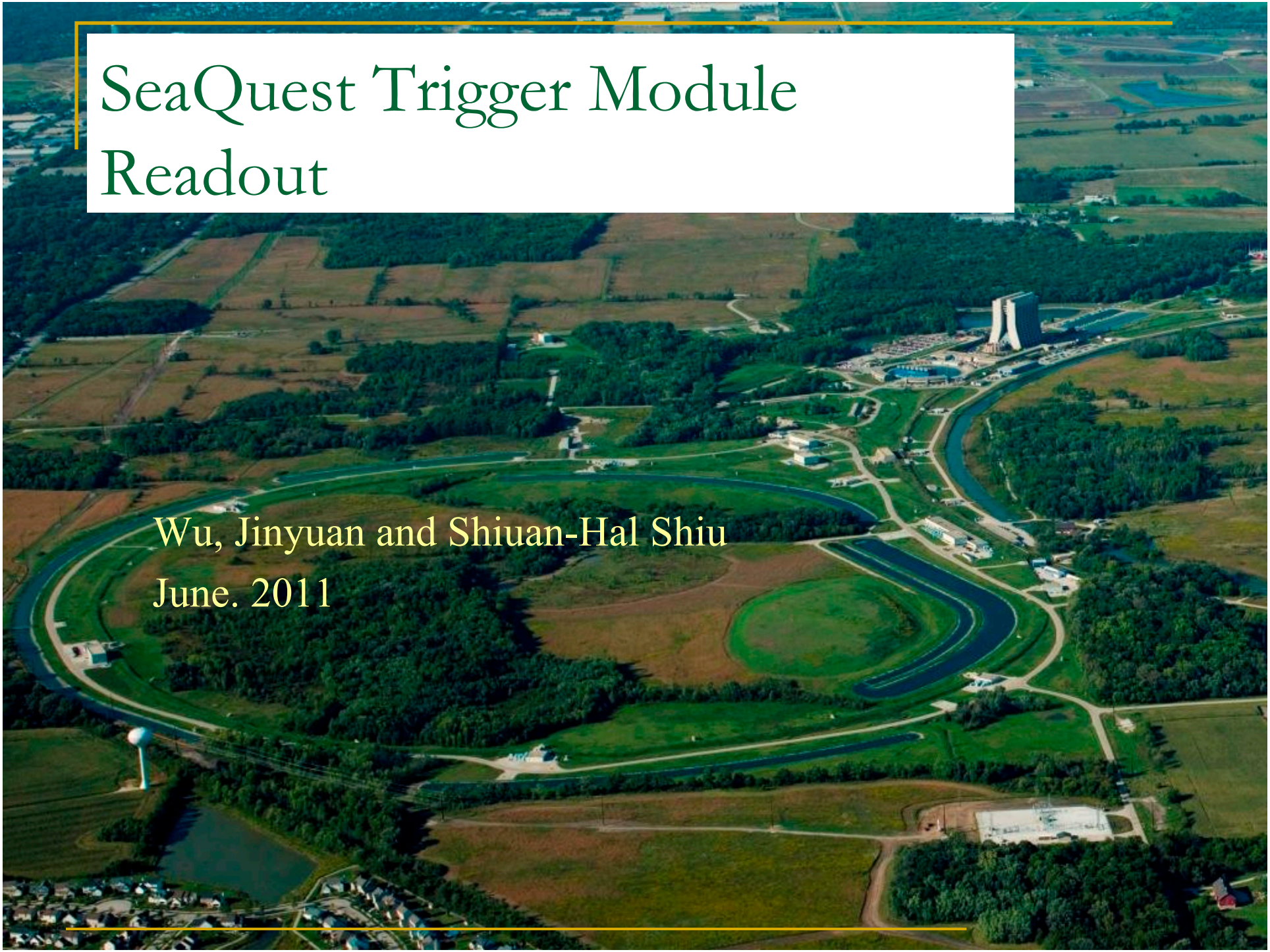
SeaQuest Trigger Module Readout



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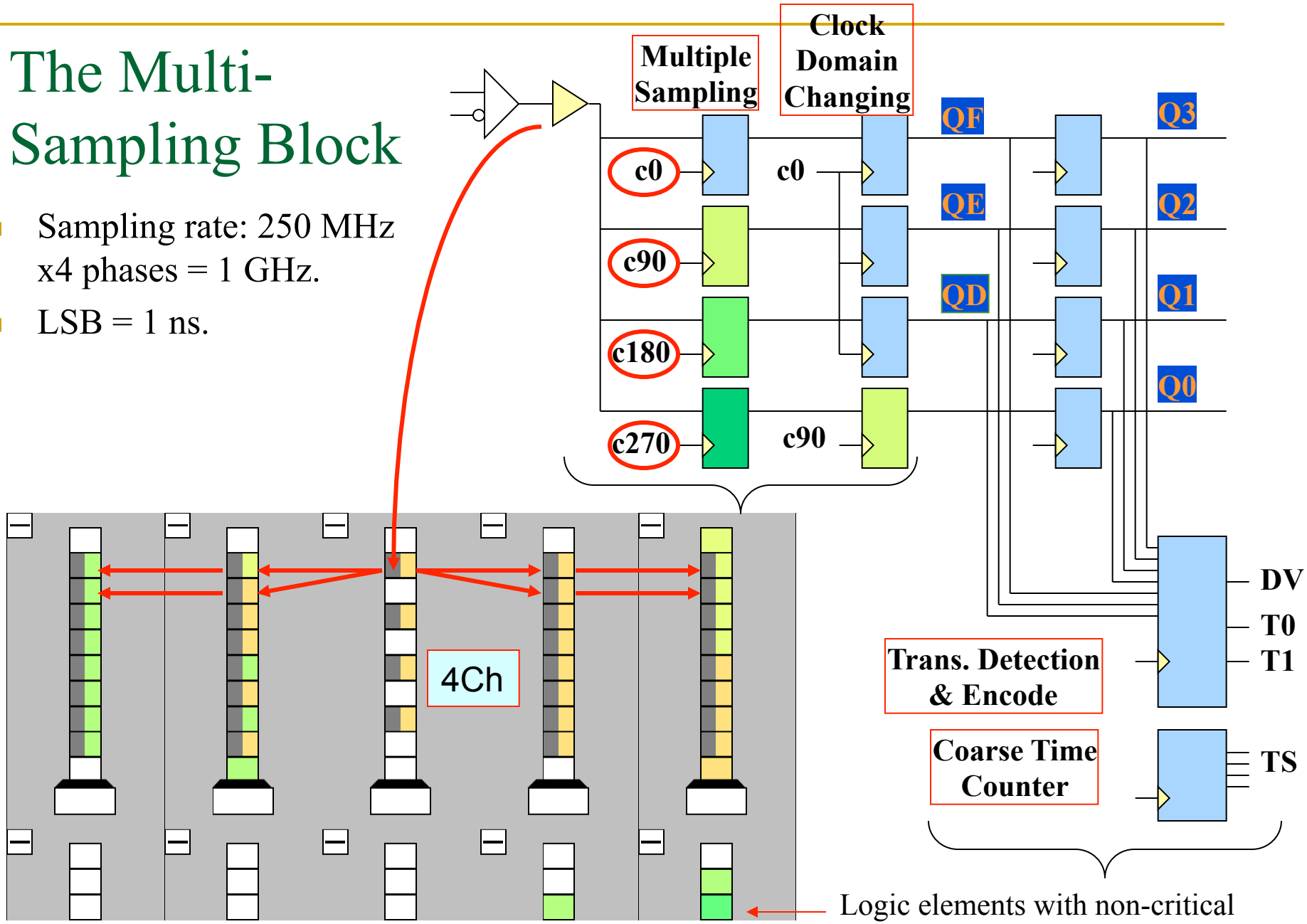
June. 2011

Introduction

- The SeaQuest Trigger modules are CAEN V1495 modules loaded with the firmware performing input transition detection, channel by channel time alignment and trigger matrix logic.
- Hit times are stored in a “latch” pipeline with 1 ns resolution, but reading out entire pipeline is not feasible due to large data volume.
- An empty time slot suppression functional block is designed inside FPGA to reduce data volume to an acceptable level.

The Multi-Sampling Block

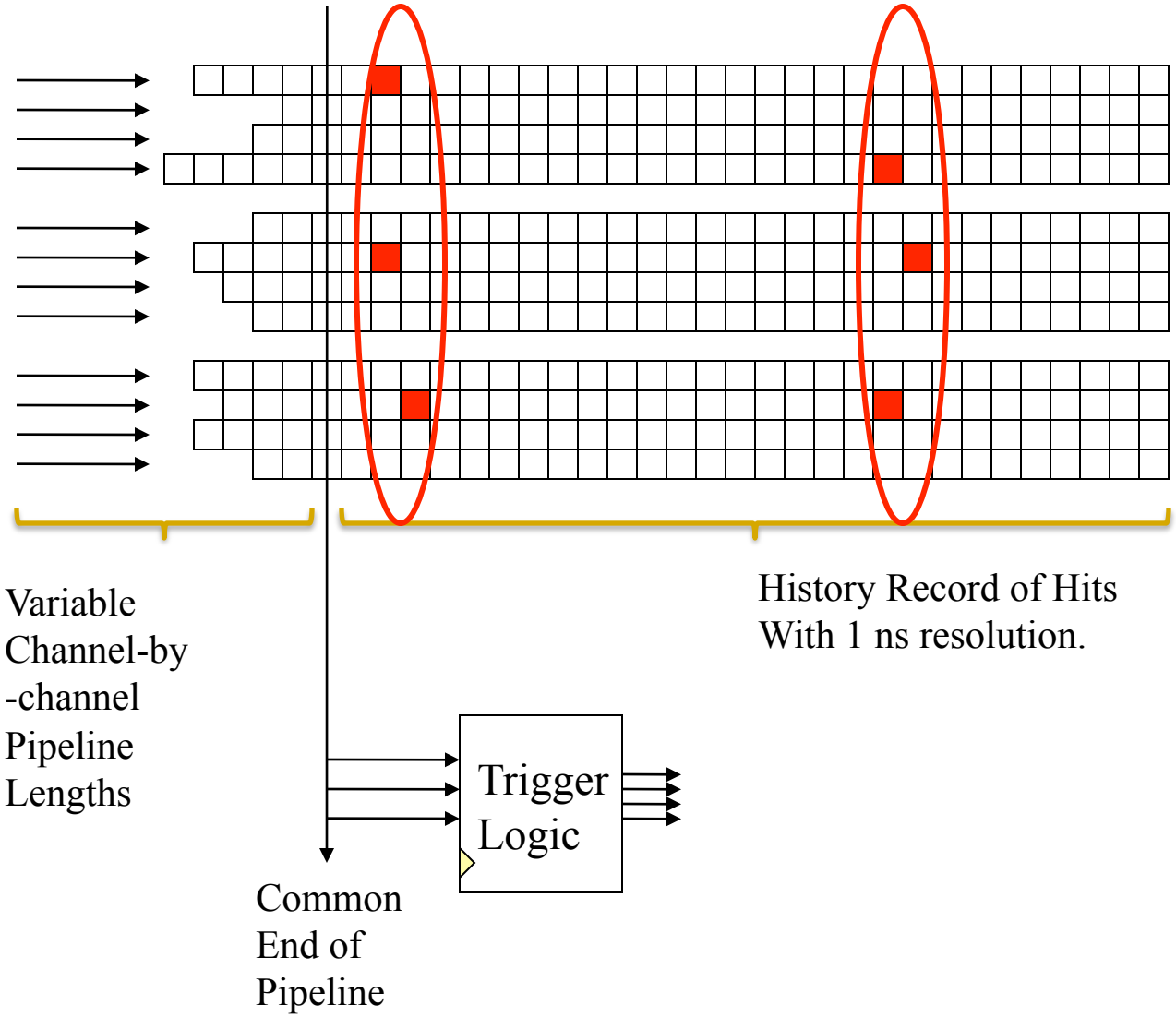
- Sampling rate: 250 MHz x4 phases = 1 GHz.
- LSB = 1 ns.



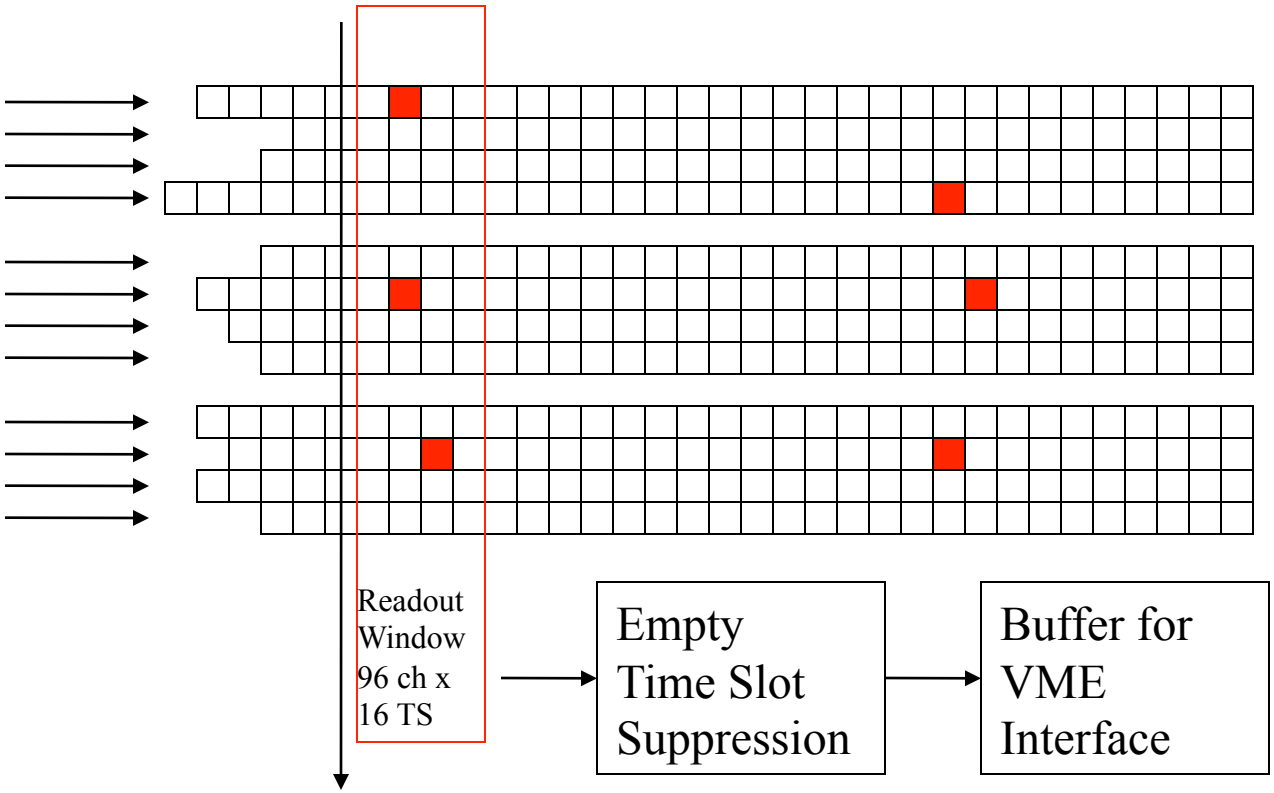
This picture represent a placement in Cyclone FPGA

Logic elements with non-critical timing are freely placed by the fitter of the compiler.

The Pipeline Structure

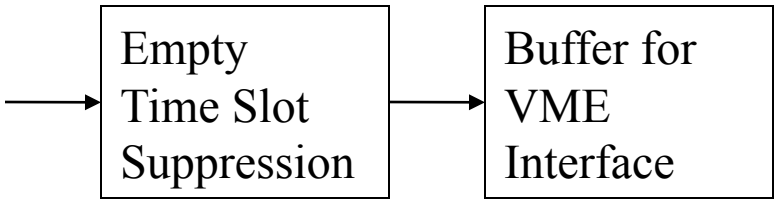


The Event Just Caused the Trigger



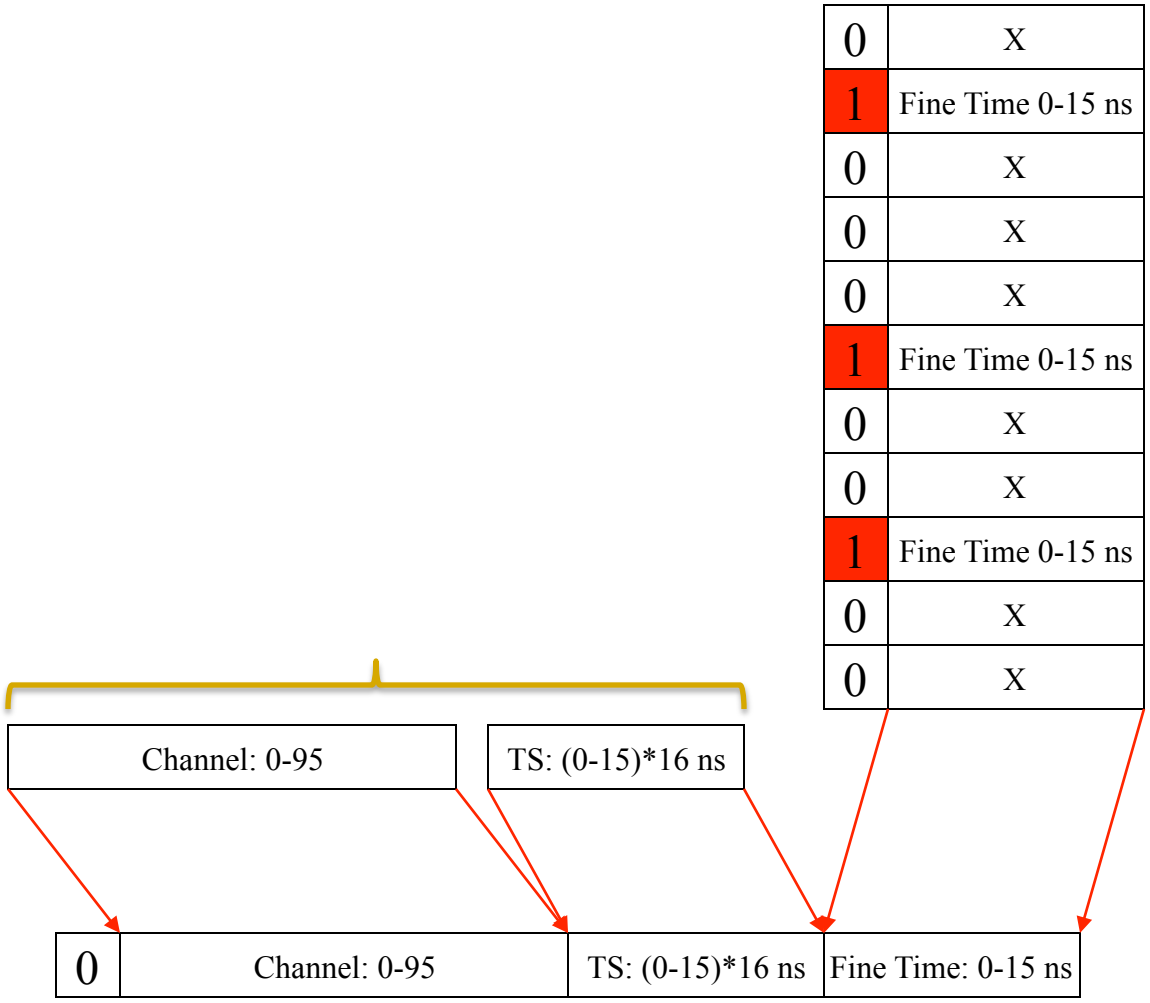
- When a trigger is generated, the pipeline stops, a history record of 16 time slots (TS) for all 96 channels will be readout. (A TS is 16 ns).
- This will generate 96*16 = 1536 words/event which is too many for VME readout.
- In reality, a lot of time slots are empty. We can suppress empty slots and readout only non-empty hits.

The Numbers Regarding Suppression



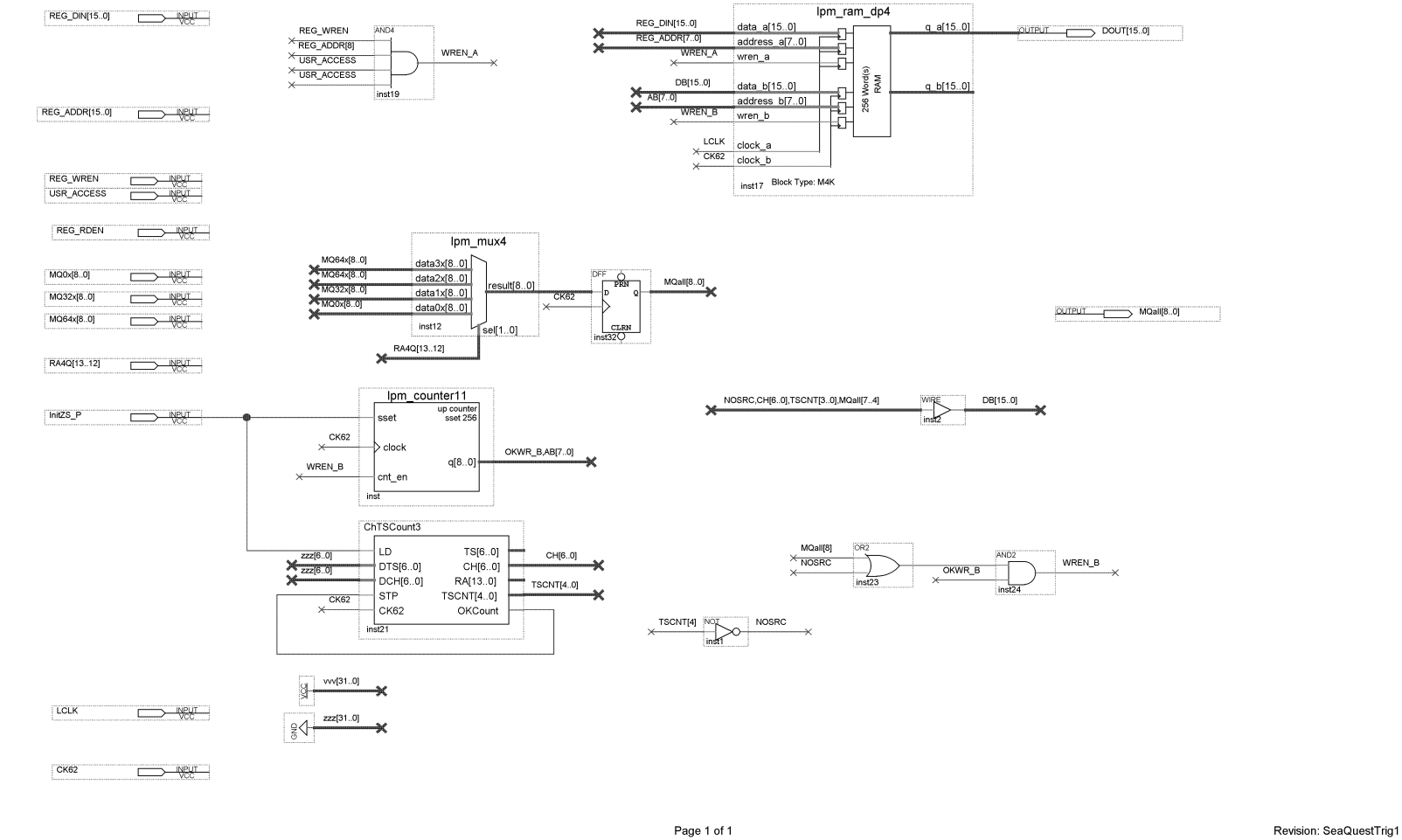
- When a trigger is generated, the pipeline stops, a history record of 16 time slots (TS) for all 96 channels i.e., 96*16 = 1536 words will be readout from the pipeline at 62.5 MHz, which takes 24.576 us.
- The buffer stores data of non-empty time slots only. The buffer capacity is 256 hits but the users can decide how many to be readout in each event.
- The readout sequence loops the hits of channels 0-95 in latest time slot first, then earlier time slots. Therefore, if there are more than 256 hits within the 16 time slots (which is unlikely), the latest hits will be readout.
- If there are less than 256 hits, the words in the buffer will be marked as end of block. The VME readout program can stop reading out additional words upon seeing the end of block mark.
- The VME readout period is < 900 ns. To readout in 5 cards a total of:
  - 512 words takes 461 us, good for up 2kHz trigger
  - 256 words takes 230 us, good for up 4kHz trigger
  - 128 words takes 115 us, good for up 8kHz trigger

The Data Format



- The empty slots do carry useful information, the channel id and time slot are implied by the order of readout. Therefore, suppressing empty hits causes the data word becomes wider.
- A 7-bit counter indicating the channel id and a 4-bit counter indicating the time slot are used to address the pipeline memory block.
- When a hit is valid (i.e., the top bit = 1), a word is written into the buffer.
- Bit 15 is the end-of-block marker:
  - =0 for regular hit
  - =1 for end-of-block

The Actual Implementation



- The previous slides are for general principles only.
- Signal-by-signal details are given in actual firmware design files.


The End
Thanks

TDC Implemented with FPGA

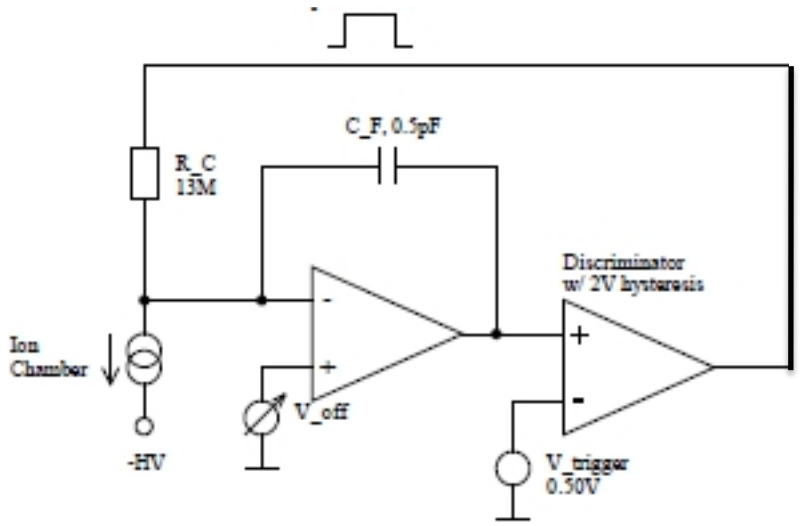
Digitization Error

- Consider a bin in a digitizer covering a range of [a, a+w]. If the input v is within [a, a+w], the input is reported to have a nominal value a+w/2. Show that for uniform distribution, the standard deviation introduced is w/sqrt(12).
- Show that if the nominal value is not a+w/2, the standard deviation will be bigger.
- Use MS Excel to generate 10000 random numbers from 0 to 1 with uniform distribution, compare the standard deviation with the theoretical number.

Ultra-wide Bins

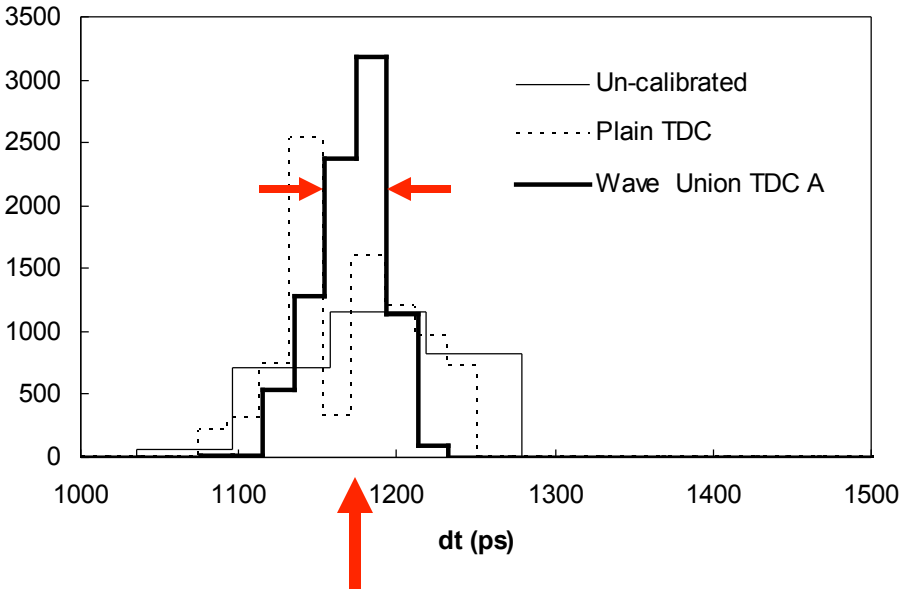
- Consider an ADC with 8 bins with widths: 3V, 1V, 1V, 1V, 1V, 1V, 1V, 1V, will the outputs of the ADC be different for inputs 4.7 and 5.7V? And for inputs 1.7 and 2.7V?
- If N input values are evenly distributed in 0 to 10V, how many measurement points will be found in each of these bins?
- For measurements in bins with width=1V and width=3V, what are the standard deviations of the measurements?
- What is the standard deviation of all measurements in entire 0 to 10V range.
- What is the equivalent bin width corresponding to the standard deviation calculated above?
- (Optional) Use MS Excel to generate 10000 random numbers from 0 to 10 with uniform distribution, compare the standard deviation with the calculated number.

Recycling Integrator

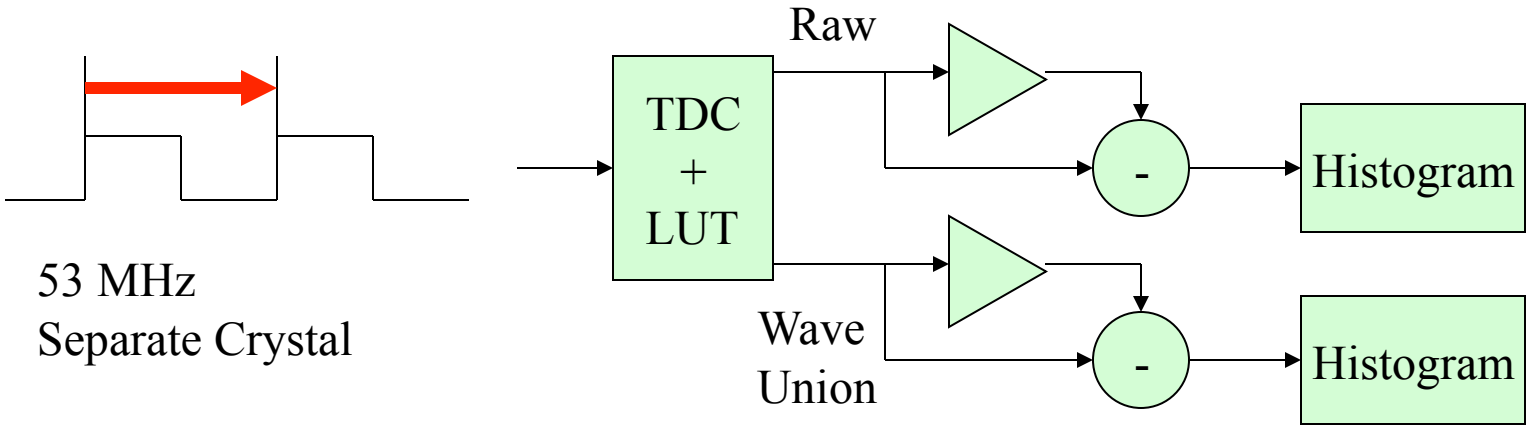


- Consider the recycling integrator above. If the charging current through R_C is 250 nA when the discriminator output is high, what are the output pulse width and interval between two pulses when the ion chamber current is 10 nA? 100 nA? 200 nA?

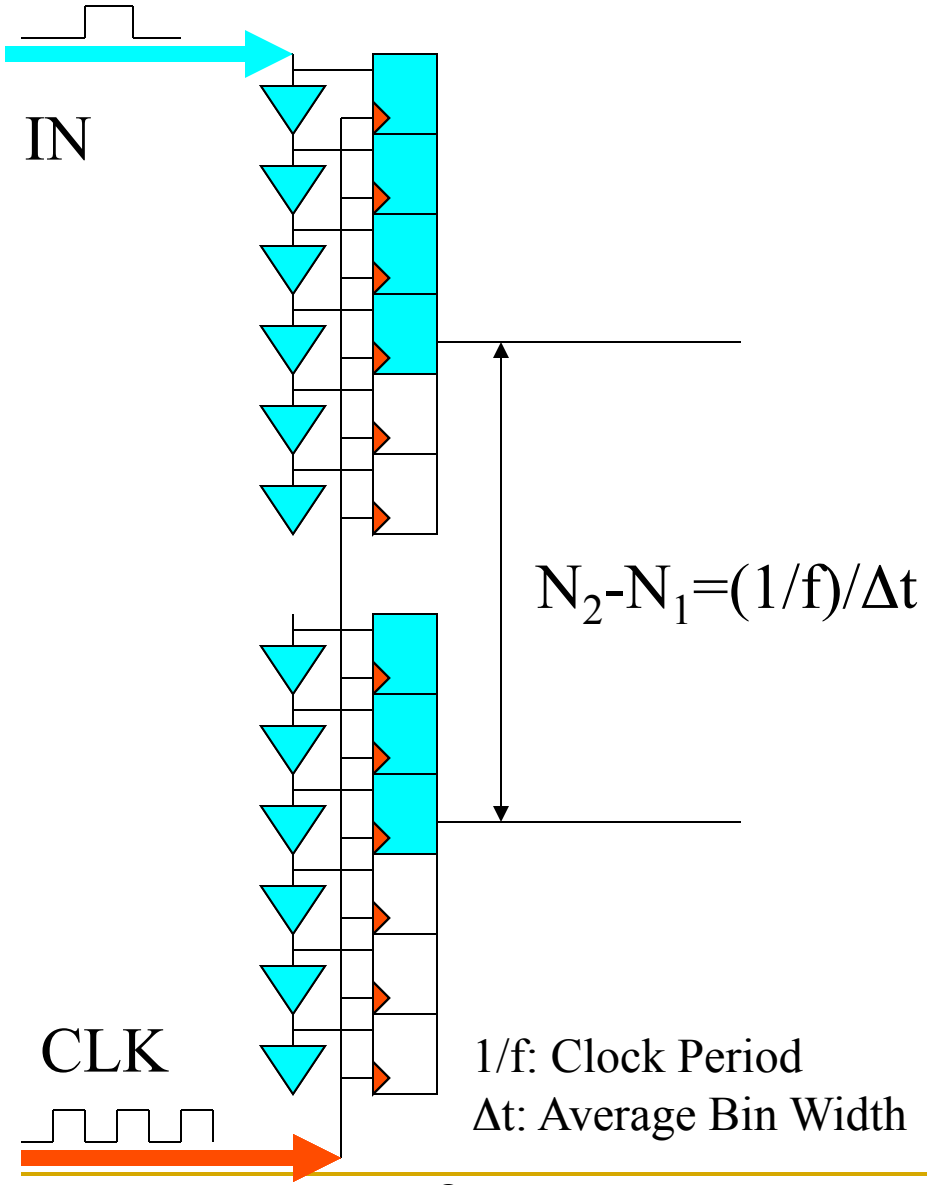
Measurement Result for Wave Union TDC A



- Plain TDC:
  - delta t RMS width: 40 ps.
  - 25 ps single hit.
- Wave Union TDC A:
  - delta t RMS width: 25 ps.
  - 17 ps single hit.



Digital Calibration Using Twice-Recording Method

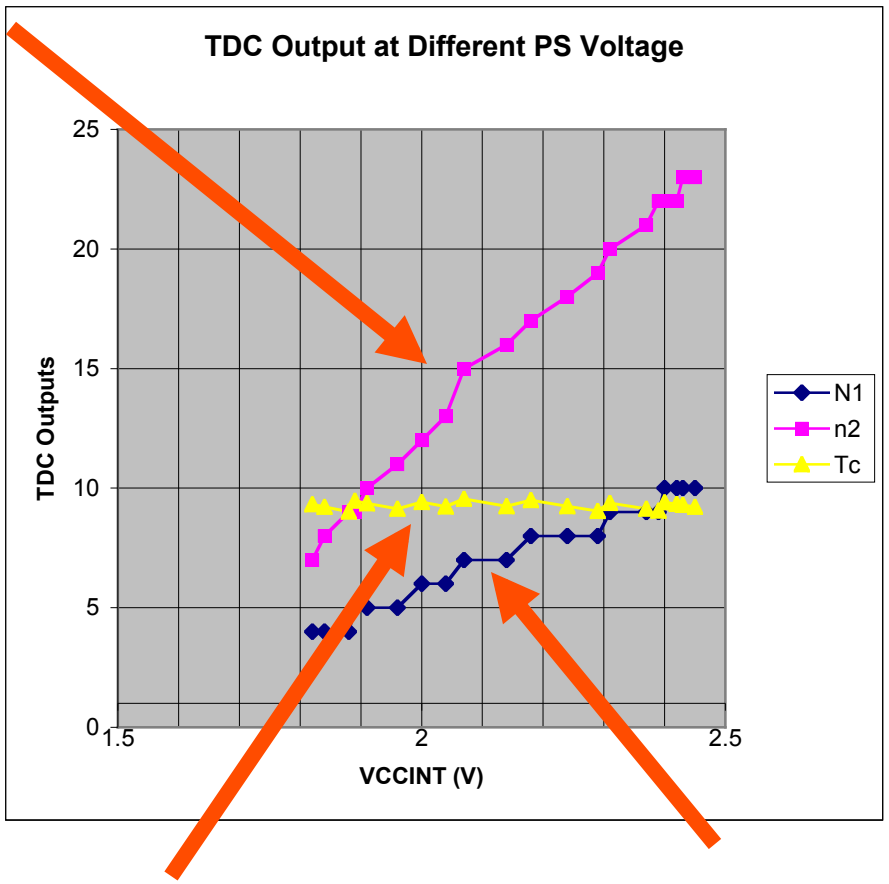


- Use longer delay line.
- Some signals may be registered twice at two consecutive clock edges.

The two measurements can be used:

- to calibrate the delay.
- to reduce digitization errors.

Digital Calibration Result

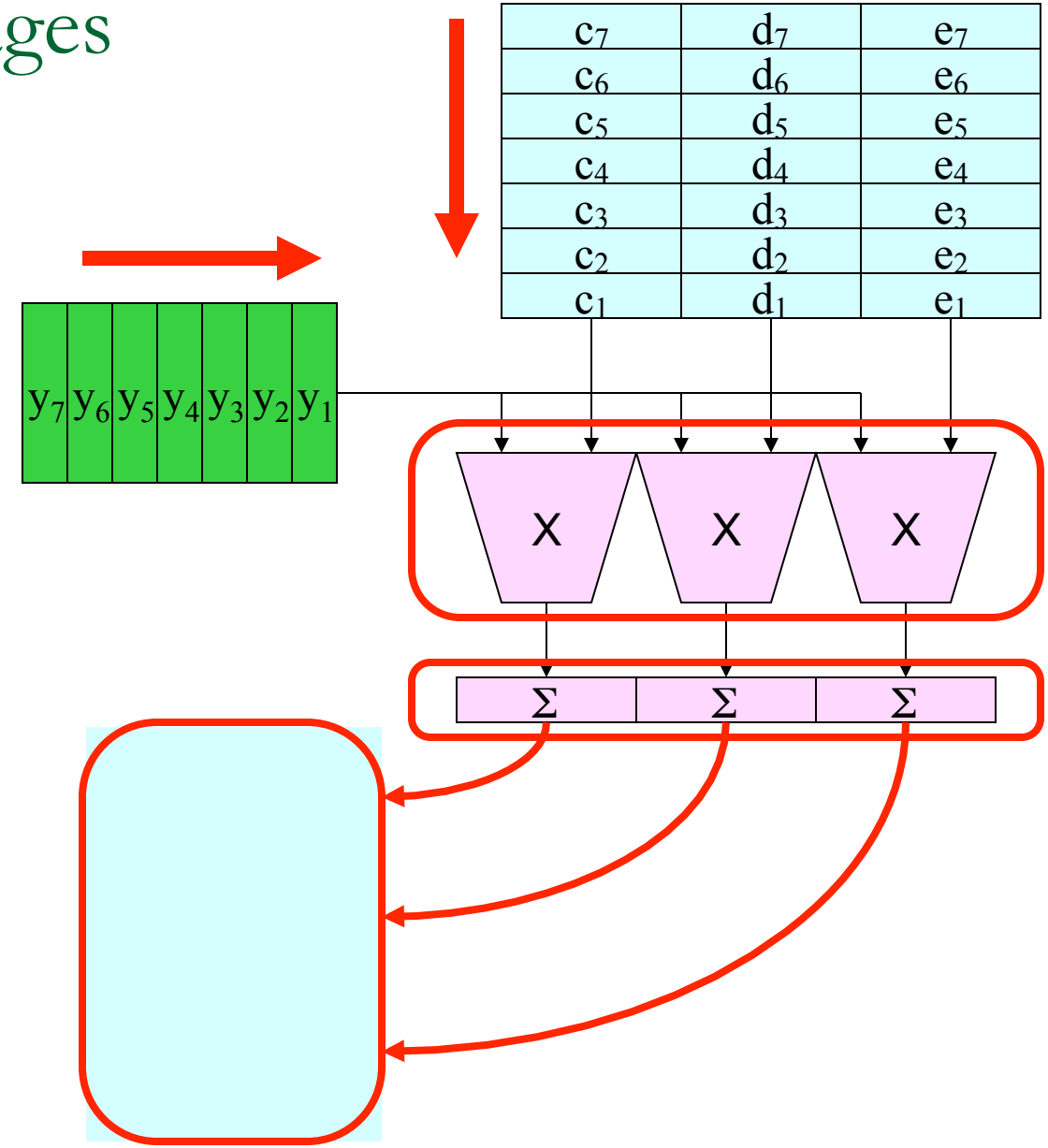


- Power supply voltage changes from 2.5 V to 1.8 V, (about the same as 100 ^{o}C to 0 ^{o}C).
- Delay speed changes by 30%.
- The difference of the two TDC numbers reflects delay speed.

- Warning: the calibration is based on average bin width, not bin-by-bin widths.

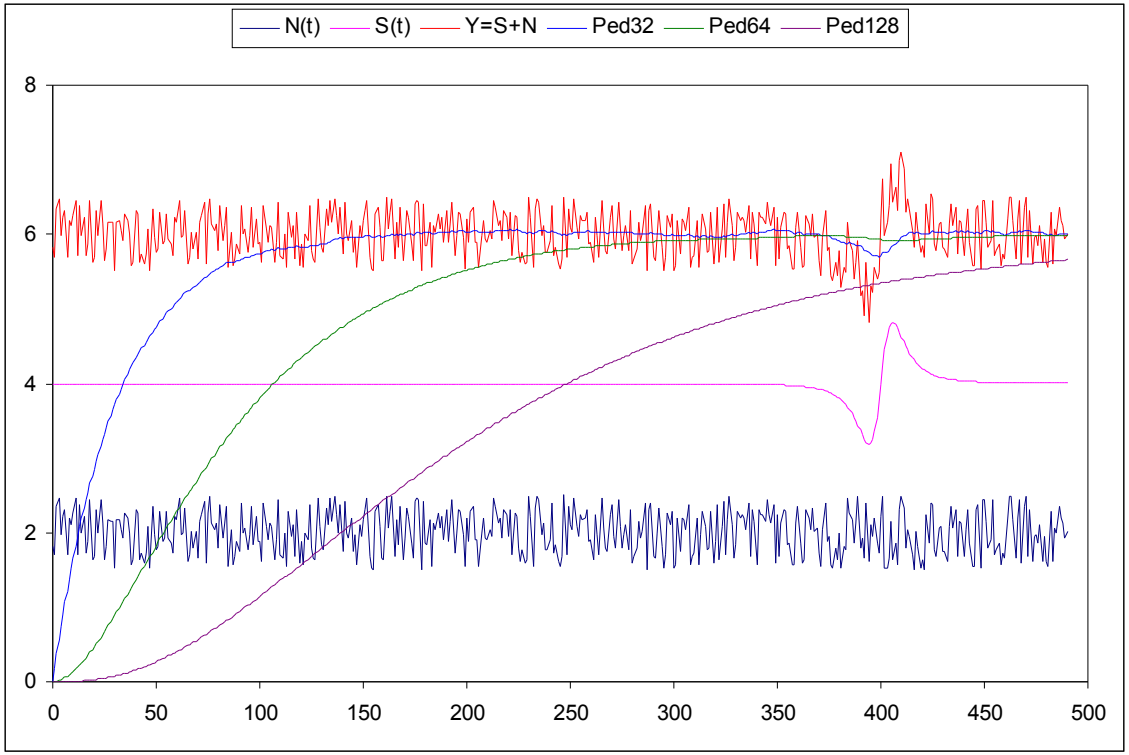
Weighted Averages

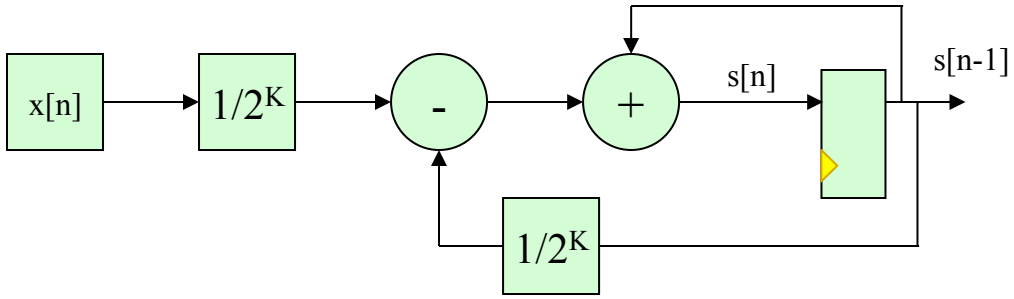
- The weighted average is a special case of inner product.
- Multipliers are usually needed.



Exponentially Weighted Average

- No multipliers are needed.
- The average is available at any time.
- It can be used to track pedestal of the input signals.





$s[n]=s[n-1]+(x[n]-s[n-1])/N$

$N=2, 4, 8, 16, 32, \ldots$